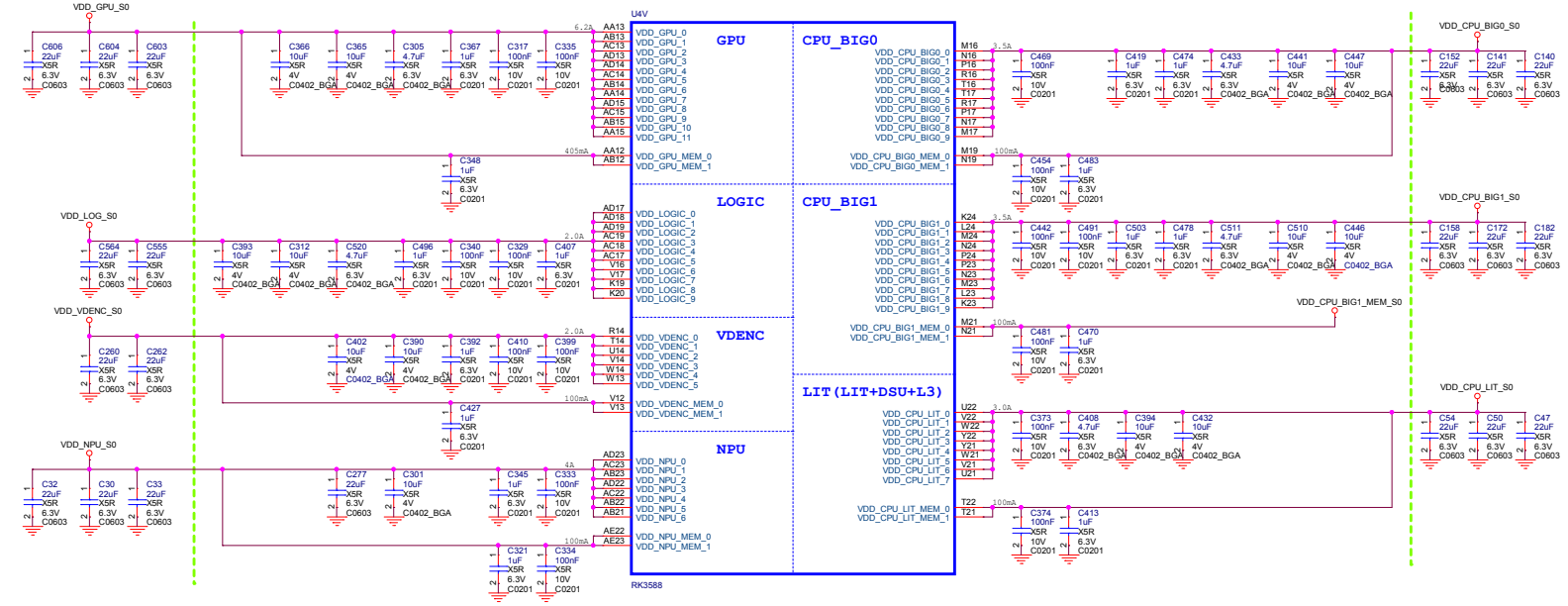
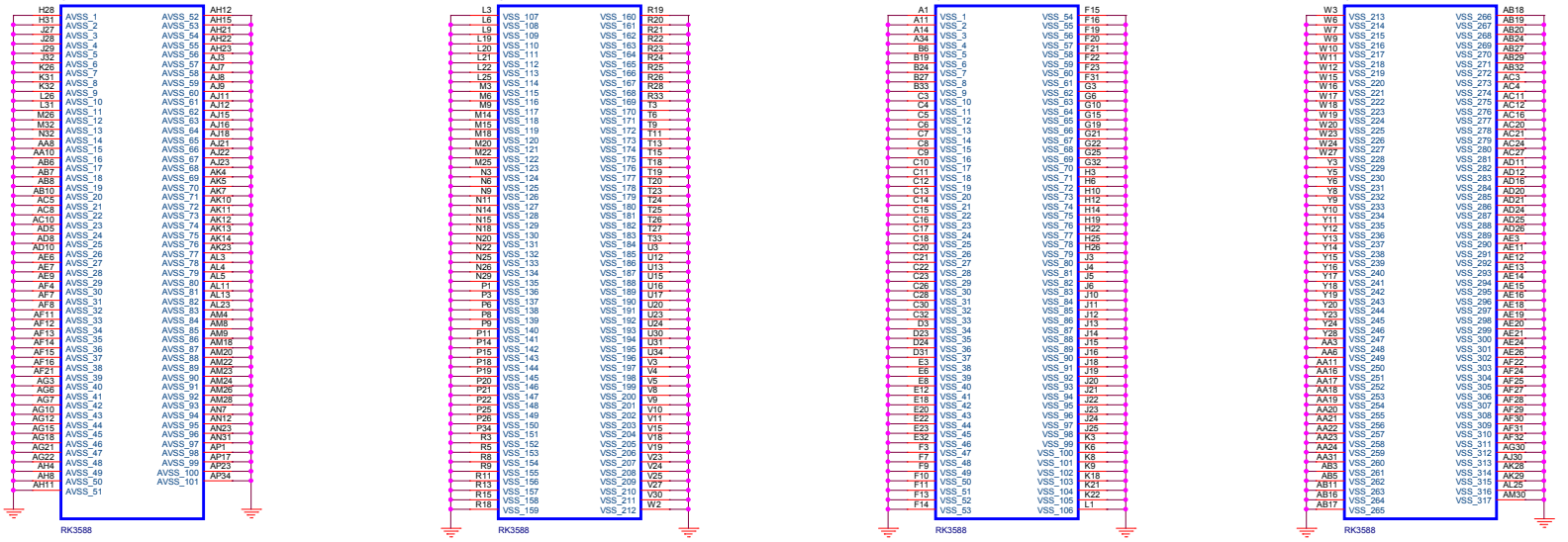
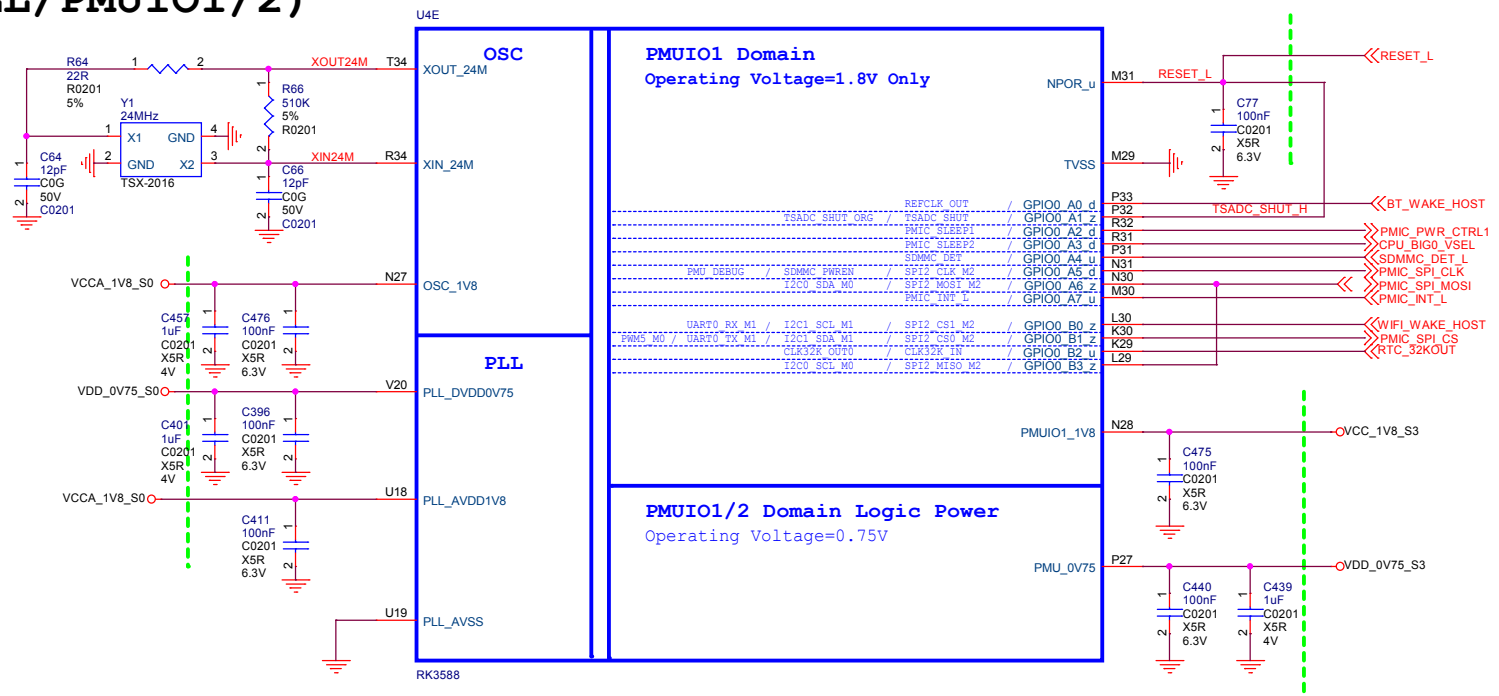
RK3588_V(POWER)

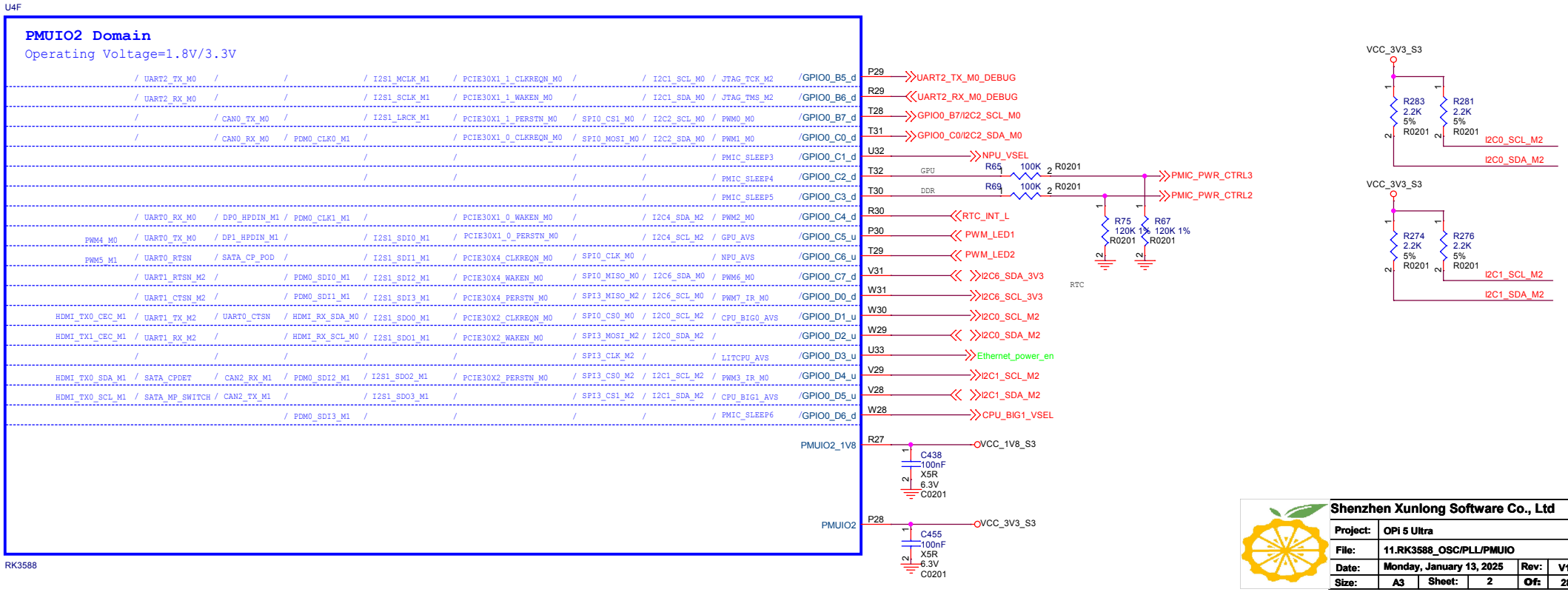




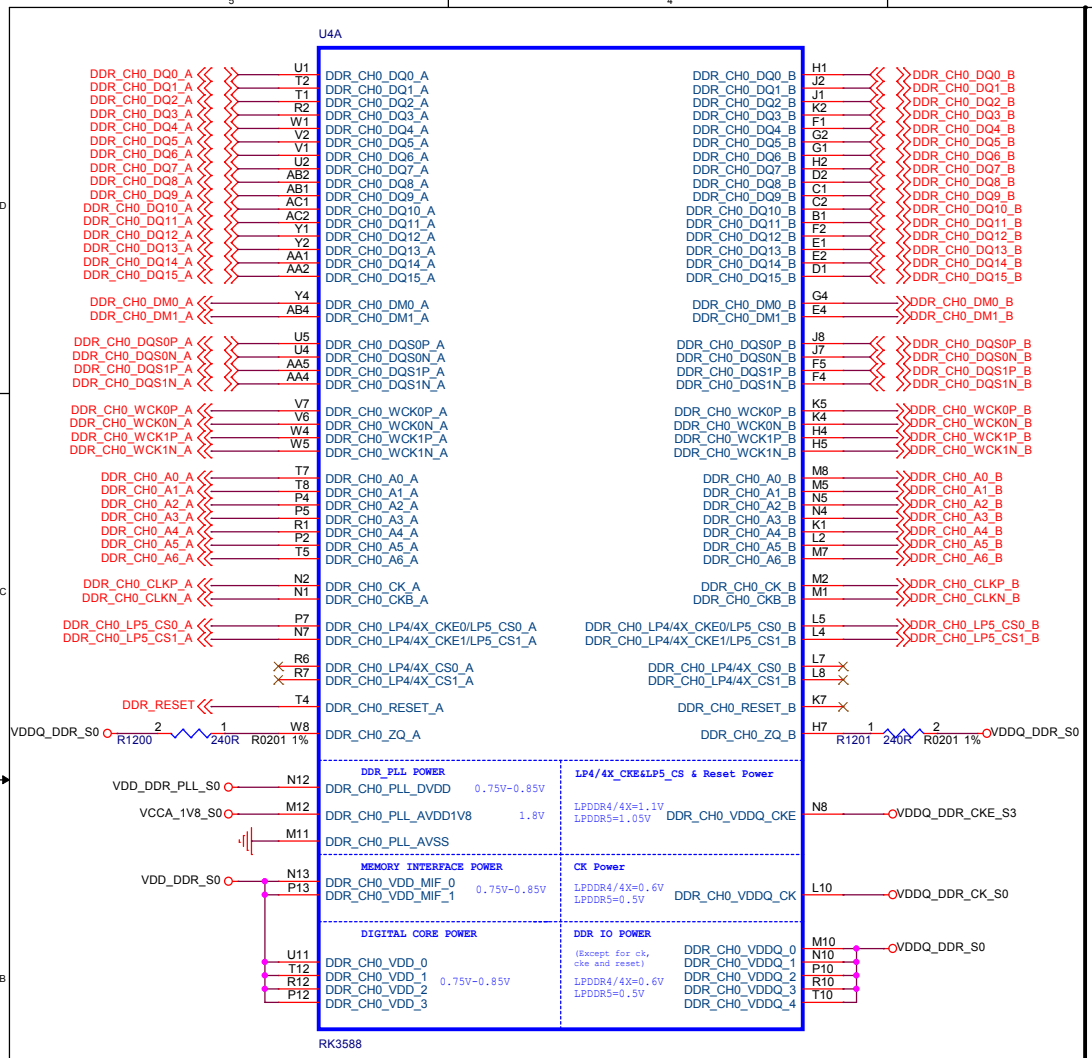
Shenzhen Xunlong Software Co., Ltd	
Project:	OPi 5 Ultra
File:	10.RK3588_Power/GND
Date:	Monday, January 13, 2025
Rev:	V1.0
Size:	A3
Sheet:	1
Of:	28

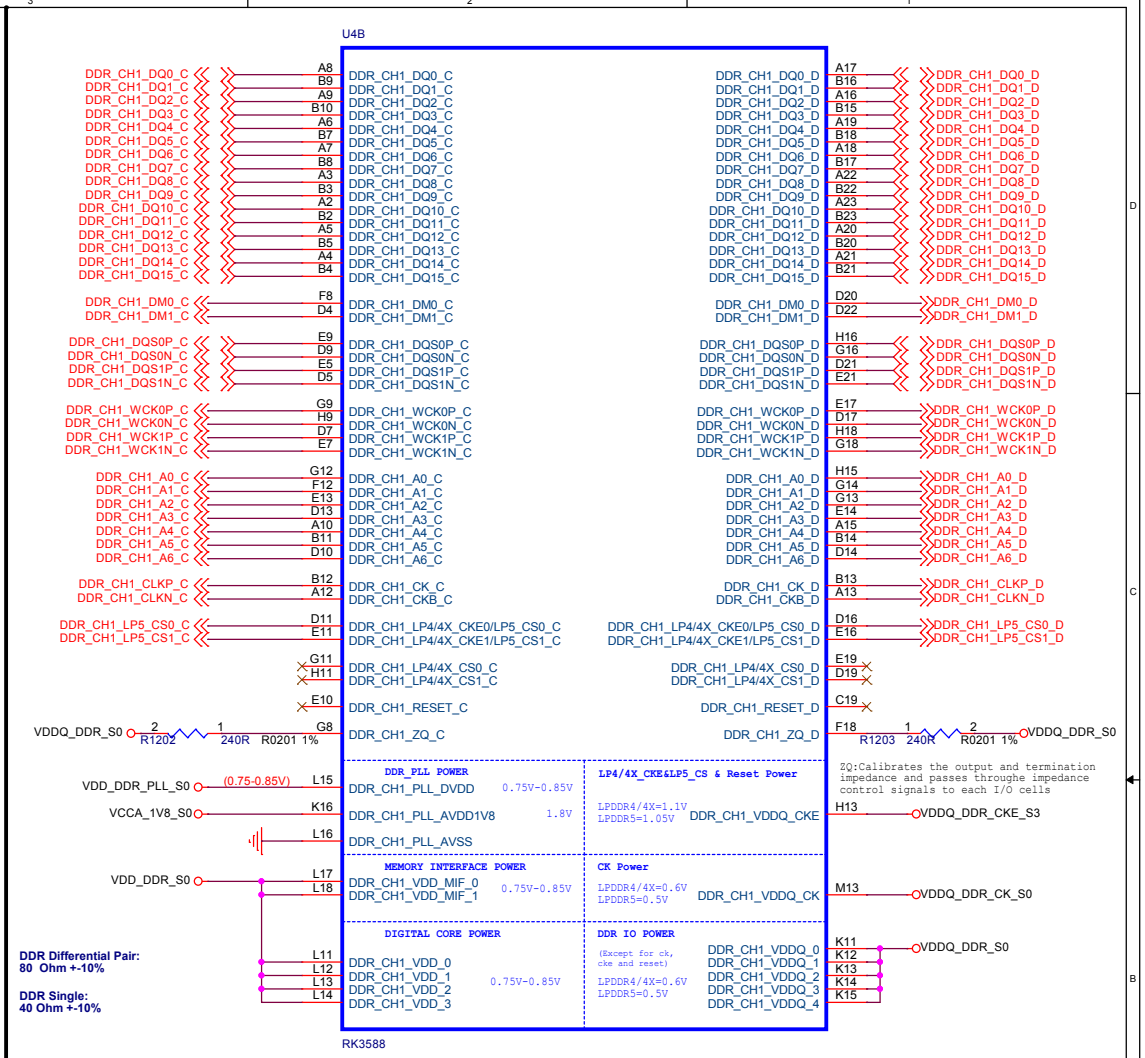
RK3588_E(OSC/PLL/PMUIO1/2)



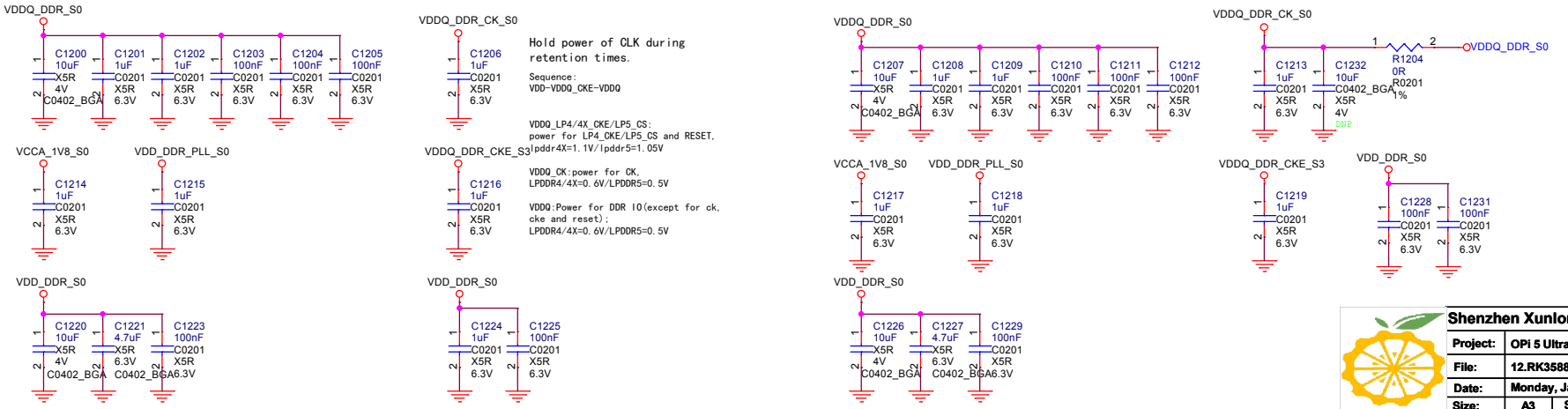


Shenzhen Xunlong Software Co., Ltd					
Project:	OPi 5 Ultra				
File:	11.RK3588_OSC/PLL/PMUIO				
Date:	Monday, January 13, 2025			Rev:	V1.0
Size:	A3	Sheet:	2	Of:	28



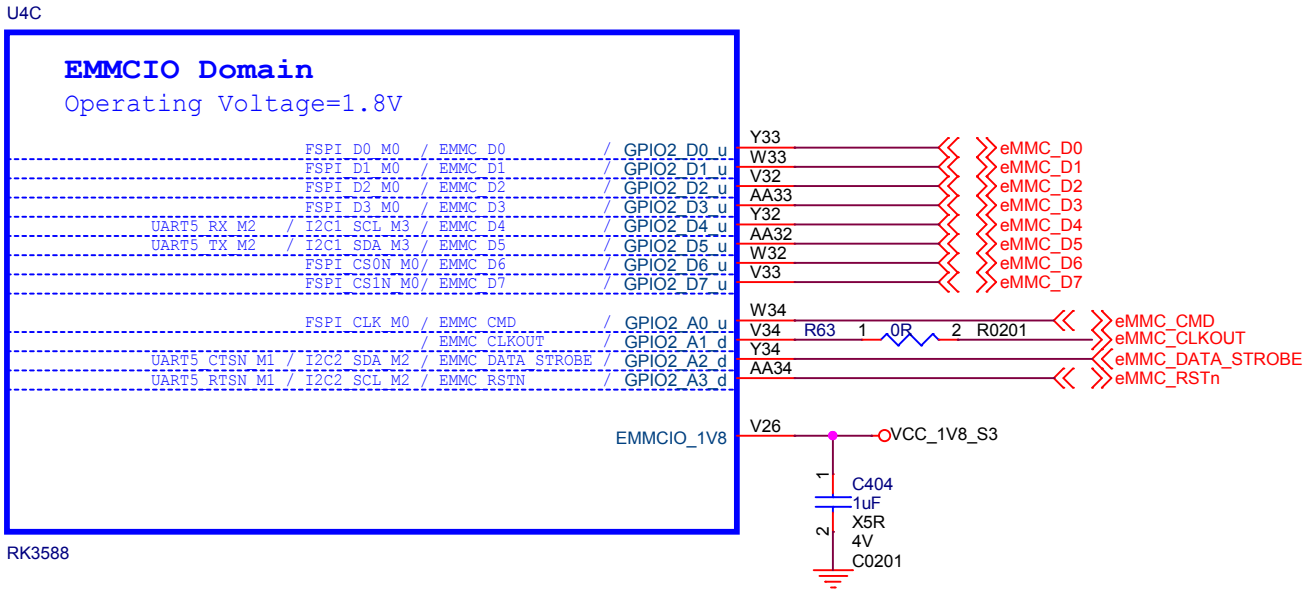


DDR FILTER

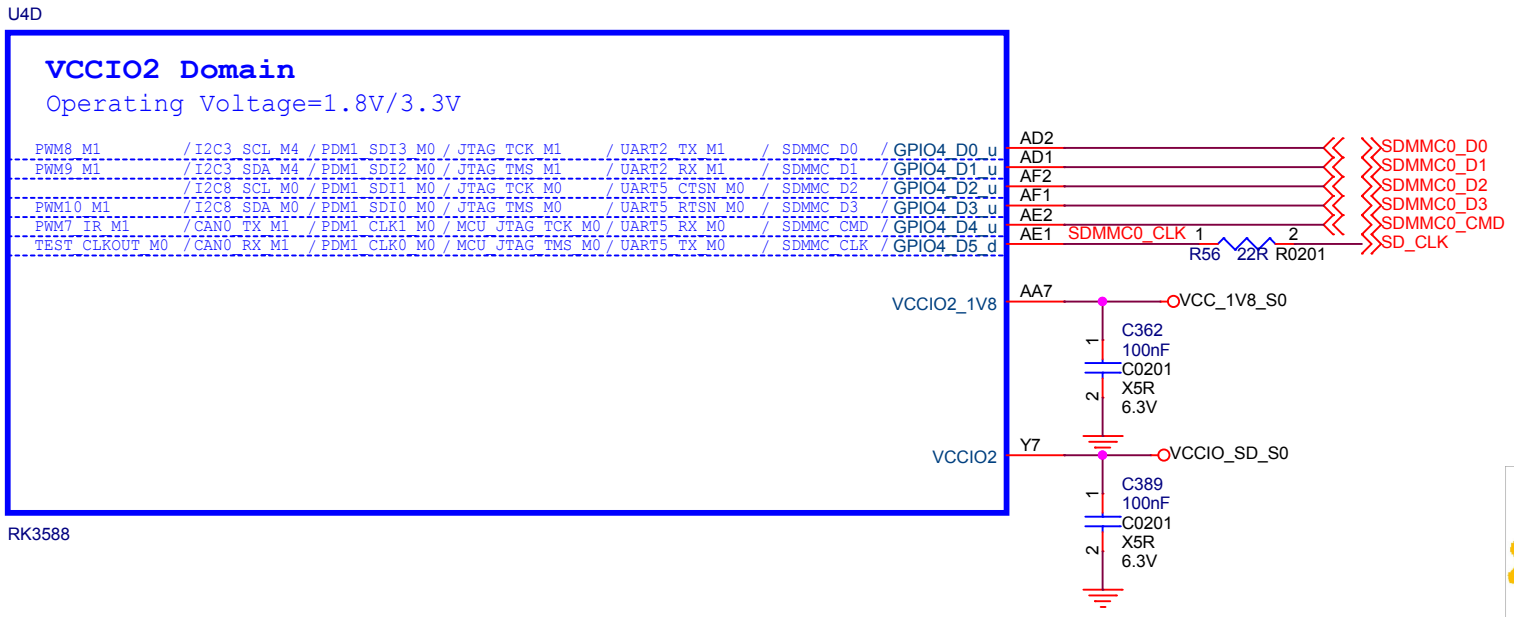


Shenzhen Xunlong Software Co., Ltd					
Project:	OPi 5 Ultra				
File:	12.RK3588 DDR Controler				
Date:	Monday, January 13, 2025			Rev:	V1.0
Size:	A3	Sheet:	3	Of:	28

RK3588_C(EMMCIO Domain)



RK3588_D(VCCIO2 Domain)



Shenzhen Xunlong Software Co., Ltd					
Project:	OPi 5 Ultra				
File:	13.RK3588_Flash/SD Controller				
Date:	Monday, January 13, 2025			Rev:	V1.0
Size:	A3	Sheet:	4	Of:	28

RK3588_M(TYPEC/DP)

U4M

USB3.0 OTG/DP1.4 Alt of TYPEC0

USB:U3/Gen1----Controller0
DP:RBR/HBR/HBR2/HBR3

TYPEC0_SBU1/DP0_AUXP — AL15
TYPEC0_SBU2/DP0_AUXN — AM15
TYPEC0_SSRX1P/DP0_TX0P — AN13 — TYPEC0_SSRX1P
TYPEC0_SSRX1N/DP0_TX0N — AP13 — TYPEC0_SSRX1N
TYPEC0_SSTX1P/DP0_TX1P — AP14 — TYPEC0_SSTX1P
TYPEC0_SSTX1N/DP0_TX1N — AN14 — TYPEC0_SSTX1N
TYPEC0_SSRX2P/DP0_TX2P — AN15
TYPEC0_SSRX2N/DP0_TX2N — AP15
TYPEC0_SSTX2P/DP0_TX3P — AP16
TYPEC0_SSTX2N/DP0_TX3N — AN16

TYPEC0_DP0_REXT — AH16 — TYPEC0_REXT — R197 1 2 8.2K R0201 1%

TYPEC0_DP0_VDD_0V85 — AJ14
TYPEC0_DP0_VDDA_0V85 — AH14 — VDDA_0V85_S0
C271 1uF X5R 6.3V C0201
C272 100nF X5R 6.3V C0201

Do not delete!!!

TYPEC0_DP0_VDDH_1V8 — AG14 — VCCA_1V8_S0
C291 1uF X5R 6.3V C0201
C289 100nF X5R 6.3V C0201

USB3.0 OTG/DP1.4 Alt of TYPEC1

USB:U3/Gen1----Controller1
DP:RBR/HBR/HBR2/HBR3

TYPEC1_SBU1/DP1_AUXP — AL10
TYPEC1_SBU2/DP1_AUXN — AM10
TYPEC1_SSRX1P/DP1_TX0P — AN8 — TYPEC1_SSRX1P
TYPEC1_SSRX1N/DP1_TX0N — AP8 — TYPEC1_SSRX1N
TYPEC1_SSTX1P/DP1_TX1P — AP9 — TYPEC1_SSTX1P
TYPEC1_SSTX1N/DP1_TX1N — AN9 — TYPEC1_SSTX1N
TYPEC1_SSRX2P/DP1_TX2P — AN10
TYPEC1_SSRX2N/DP1_TX2N — AP10
TYPEC1_SSTX2P/DP1_TX3P — AP11
TYPEC1_SSTX2N/DP1_TX3N — AN11

TYPEC1_DP1_REXT — AG16 — TYPEC1_REXT — R200 8.2K R0201

TYPEC1_DP1_VDD_0V85 — AH13
TYPEC1_DP1_VDDA_0V85 — AJ13 — VDDA_0V85_S0
C270 1uF X5R 6.3V C0201
C273 100nF X5R 6.3V C0201

TYPEC1_DP1_VDDH_1V8 — AG13 — VCCA_1V8_S0
C292 1uF X5R 6.3V C0201
C293 100nF X5R 6.3V C0201

RK3588

RK3588_L(USB2.0 HOST/OTG)

U4L

USB2.0 of TYPEC0 (OTG/HOST/DEVICE)

HS/FS/LS

Download Port

TYPEC0_USB20_OTG_DP — AL12 — TYPEC0_OTG_DP
TYPEC0_USB20_OTG_DM — AM12 — TYPEC0_OTG_DM
TYPEC0_USB20_OTG_ID — AL14
TYPEC0_USB20_VBUSDET — 40K — AM14 — TYPEC0_USB20_VBUSDET
TYPEC0_USB20_OTG0_REXT — AP12 — OTG0_REXT — R41 200R R0201

USB20 Differential Pair:
DATE:90 Ohm +-10%

USB2.0 of TYPEC1 (OTG/HOST/DEVICE)

HS/FS/LS

TYPEC1_USB20_OTG_DP — AK9 — TYPEC1_OTG_DP
TYPEC1_USB20_OTG_DM — AL9 — TYPEC1_OTG_DM
TYPEC1_USB20_OTG_ID — AK8
to USB3.0
TYPEC1_USB20_VBUSDET — 40K — AL8
TYPEC1_USB20_OTG1_REXT — AP7 — OTG1_REXT — R40 200R R0201

USB2.0 HOST0

HS/FS/LS

USB20_HOST0_DP — AK6 — USB20_HOST0_DP
USB20_HOST0_DM — AL6 — USB20_HOST0_DM
to USB2.0
USB20_HOST0_REXT — AG9 — HOST0_REXT — R201 200R R0201

USB2.0 HOST1

HS/FS/LS

USB20_HOST1_DP — AL7 — USB20_HOST1_DP
USB20_HOST1_DM — AM7 — USB20_HOST1_DM
to USB2.0
USB20_HOST1_REXT — AH9 — HOST1_REXT — R195 200R R0201

USB2.0 POWER

USB20_DVDD_0V75 — AH10 — VDD_0V75_S0
C281 100nF X5R 6.3V C0201

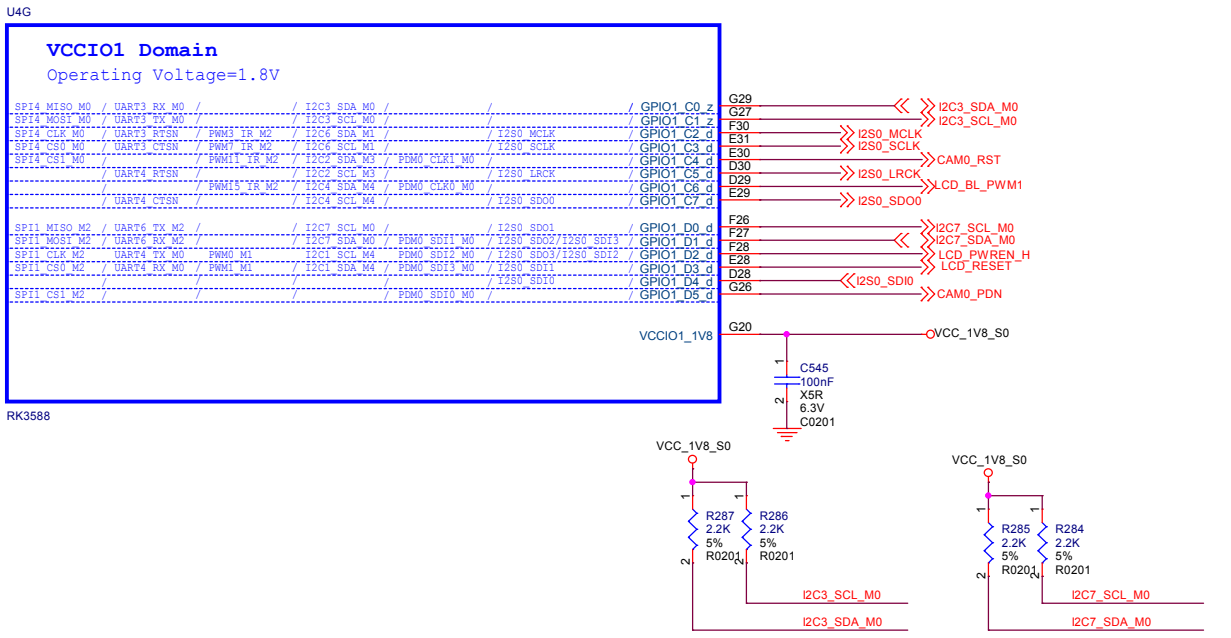
USB20_AVDD_1V8 — AG11 — VCCA_1V8_S0
C290 100nF X5R 6.3V C0201

USB20_AVDD_3V3 — AJ10 — VCCA_3V3_S0
C267 100nF X5R 6.3V C0201

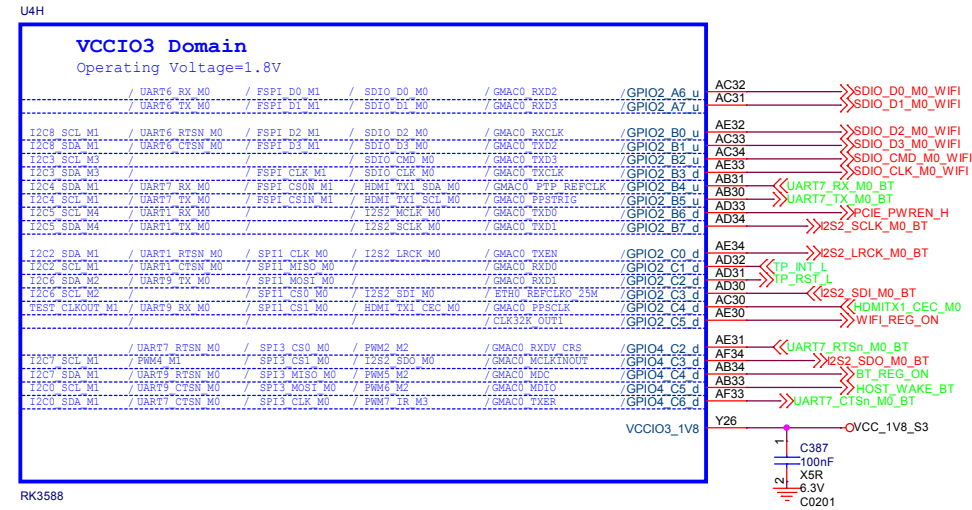
RK3588

Shenzhen Xunlong Software Co., Ltd					
Project:	OPi 5 Ultra				
File:	14.RK3588_USB30/USB20_Ctrl				
Date:	Monday, January 13, 2025			Rev:	V1.0
Size:	A3	Sheet:	5	Of:	28

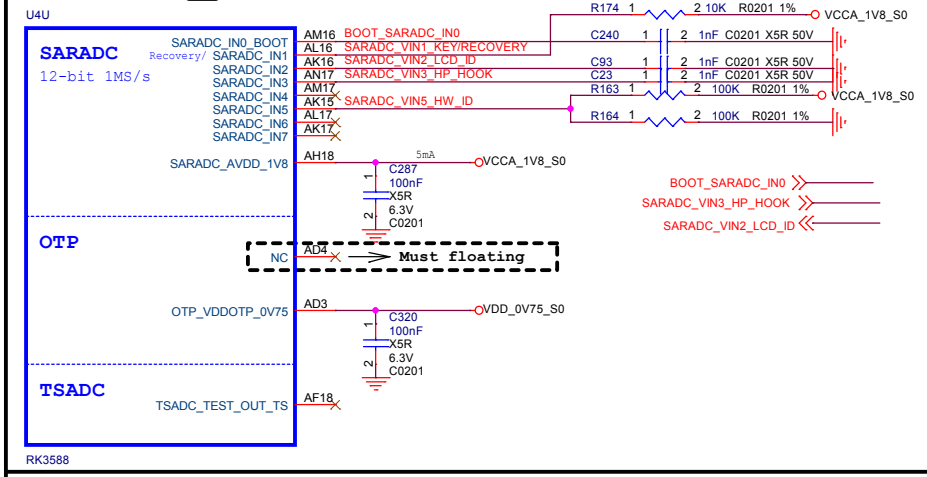
RK3588_G(VCCIO1 Domain)



RK3588_H(VCCIO3 Domain)



RK3588_U(SARADC/OTP)



BOOT MODE CONFIG

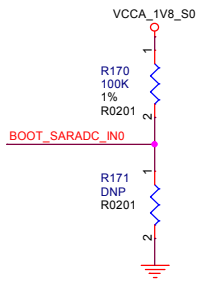


TABLE 1

Item	Rup	Rdown	ADC	VOL	BOOT MODE
LEVEL1	DNP	100K	0	0V	USB (Maskrom mode)
LEVEL2	100K	20K	682	0.3V	SD Card-USB
LEVEL3	100K	51K	1365	0.6V	EMMC-USB
LEVEL4	100K	100K	2047	0.9V	FSPI M0-USB
LEVEL5	100K	200K	2730	1.2V	FSPI M1-USB
LEVEL6	100K	499K	3412	1.5V	FSPI M2-USB
LEVEL7	100K	DNP	4095	1.8V	FSPI_M2-FSPI_M1-FSPI_M0 -EMMC-SD Card-USB

Shenzhen Xunlong Software Co., Ltd					
Project:	OPi 5 Ultra				
File:	15.RK3588_SARADC/1.8V Only GPIO				
Date:	Monday, January 13, 2025			Rev:	V1.0
Size:	A3	Sheet:	6	Of:	28

RK3588_Q/R(MIPI_D/C_PHY0/1)

U4Q

MIPI D/C-PHY DSI_TX Port0

D-PHY:V2.0 4.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

MIPI_DPHY0_TX_CLKP/MIPI_CPHY0_TX_TRIO1_C	AN26
MIPI_DPHY0_TX_CLKN/MIPI_CPHY0_TX_TRIO1_B	AP26
MIPI_DPHY0_TX_D0P/MIPI_CPHY0_TX_TRIO0_B	AN24
MIPI_DPHY0_TX_D0N/MIPI_CPHY0_TX_TRIO0_A	AP24
MIPI_DPHY0_TX_D1P/MIPI_CPHY0_TX_TRIO1_A	AN25
MIPI_DPHY0_TX_D1N/MIPI_CPHY0_TX_TRIO0_C	AP25
MIPI_DPHY0_TX_D2P/MIPI_CPHY0_TX_TRIO2_B	AN27
MIPI_DPHY0_TX_D2N/MIPI_CPHY0_TX_TRIO2_A	AP27
MIPI_DPHY0_TX_D3P/NO_USE_AN28	AN28
MIPI_DPHY0_TX_D3N/MIPI_CPHY0_TX_TRIO2_C	AP28

MIPI D/C-PHY CSI_RX Port0

D-PHY:V1.2 2.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

Note:
此D-PHY使用受限!!!
详细情况请参阅硬件
设计指南。
This D-PHY is limited!!!
Please refer to the
hardware design guide
for details.

MIPI_DPHY0_RX_CLKP/MIPI_CPHY0_RX_TRIO1_C	AN32	MIPI_DPHY0_RX_CLKP
MIPI_DPHY0_RX_CLKN/MIPI_CPHY0_RX_TRIO1_B	AP31	MIPI_DPHY0_RX_CLKN
MIPI_DPHY0_RX_D0P/MIPI_CPHY0_RX_TRIO0_B	AN29	MIPI_DPHY0_RX_D0P
MIPI_DPHY0_RX_D0N/MIPI_CPHY0_RX_TRIO0_A	AP29	MIPI_DPHY0_RX_D0N
MIPI_DPHY0_RX_D1P/MIPI_CPHY0_RX_TRIO1_A	AN30	MIPI_DPHY0_RX_D1P
MIPI_DPHY0_RX_D1N/MIPI_CPHY0_RX_TRIO0_C	AP30	MIPI_DPHY0_RX_D1N
MIPI_DPHY0_RX_D2P/MIPI_CPHY0_RX_TRIO2_B	AN33	MIPI_DPHY0_RX_D2P
MIPI_DPHY0_RX_D2N/MIPI_CPHY0_RX_TRIO2_A	AP32	MIPI_DPHY0_RX_D2N
MIPI_DPHY0_RX_D3P/NO_USE_AN34	AN34	MIPI_DPHY0_RX_D3P
MIPI_DPHY0_RX_D3N/MIPI_CPHY0_RX_TRIO2_C	AP33	MIPI_DPHY0_RX_D3N

MIPI D/C-PHY POWER

MIPI_D/C_PHY0_VREG	AF20	C304 1uF	1 2 C0201 X5R 4V
MIPI_D/C_PHY0_VDD	AG20	C286 100nF X5R 6.3V C0201 / C285 1uF X5R 6.3V C0201	VDD_0V75_S0
MIPI_D/C_PHY0_VDD_1V2	AH20	C278 1uF X5R 6.3V C0201	VDDA_1V2_S0
MIPI_D/C_PHY0_VDD_1V8	AJ20	C268 1uF X5R 6.3V C0201	VCC_1V8_S0

RK3588

U4R

MIPI D/C-PHY DSI_TX Port1

D-PHY:V2.0 4.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

MIPI_DPHY1_TX_CLKP/MIPI_CPHY1_TX_TRIO1_C	AN20
MIPI_DPHY1_TX_CLKN/MIPI_CPHY1_TX_TRIO1_B	AP20
MIPI_DPHY1_TX_D0P/MIPI_CPHY1_TX_TRIO0_B	AN18
MIPI_DPHY1_TX_D0N/MIPI_CPHY1_TX_TRIO0_A	AP18
MIPI_DPHY1_TX_D1P/MIPI_CPHY1_TX_TRIO1_A	AN19
MIPI_DPHY1_TX_D1N/MIPI_CPHY1_TX_TRIO0_C	AP19
MIPI_DPHY1_TX_D2P/MIPI_CPHY1_TX_TRIO2_B	AN21
MIPI_DPHY1_TX_D2N/MIPI_CPHY1_TX_TRIO2_A	AP21
MIPI_DPHY1_TX_D3P /NO_USE_AN22	AN22
MIPI_DPHY1_TX_D3N/MIPI_CPHY1_TX_TRIO2_C	AP22

MIPI_DPHY1_TX_CLKP	MIPI_DPHY1_TX_CLKP
MIPI_DPHY1_TX_CLKN	MIPI_DPHY1_TX_CLKN
MIPI_DPHY1_TX_D0P	MIPI_DPHY1_TX_D0P
MIPI_DPHY1_TX_D0N	MIPI_DPHY1_TX_D0N
MIPI_DPHY1_TX_D1P	MIPI_DPHY1_TX_D1P
MIPI_DPHY1_TX_D1N	MIPI_DPHY1_TX_D1N
MIPI_DPHY1_TX_D2P	MIPI_DPHY1_TX_D2P
MIPI_DPHY1_TX_D2N	MIPI_DPHY1_TX_D2N
MIPI_DPHY1_TX_D3P	MIPI_DPHY1_TX_D3P
MIPI_DPHY1_TX_D3N	MIPI_DPHY1_TX_D3N

MIPI D/C-PHY CSI_RX Port1

D-PHY:V1.2 2.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

Note:
此D-PHY使用受限!!!
详细情况请参阅硬件
设计指南。
This D-PHY is limited!!!
Please refer to the
hardware design guide
for details.

MIPI_DPHY1_RX_CLKP/MIPI_CPHY1_RX_TRIO1_C	AK20	MIPI_DPHY1_RX_CLKP
MIPI_DPHY1_RX_CLKN/MIPI_CPHY1_RX_TRIO1_B	AL20	MIPI_DPHY1_RX_CLKN
MIPI_DPHY1_RX_D0P/MIPI_CPHY1_RX_TRIO0_B	AK18	MIPI_DPHY1_RX_D0P
MIPI_DPHY1_RX_D0N/MIPI_CPHY1_RX_TRIO0_A	AL18	MIPI_DPHY1_RX_D0N
MIPI_DPHY1_RX_D1P/MIPI_CPHY1_RX_TRIO1_A	AK19	MIPI_DPHY1_RX_D1P
MIPI_DPHY1_RX_D1N/MIPI_CPHY1_RX_TRIO0_C	AL19	MIPI_DPHY1_RX_D1N
MIPI_DPHY1_RX_D2P/MIPI_CPHY1_RX_TRIO2_B	AK21	MIPI_DPHY1_RX_D2P
MIPI_DPHY1_RX_D2N/MIPI_CPHY1_RX_TRIO2_A	AL21	MIPI_DPHY1_RX_D2N
MIPI_DPHY1_RX_D3P/NO_USE_AK22	AK22	MIPI_DPHY1_RX_D3P
MIPI_DPHY1_RX_D3N/MIPI_CPHY1_RX_TRIO2_C	AL22	MIPI_DPHY1_RX_D3N

MIPI D/C-PHY POWER

MIPI_D/C_PHY1_VREG	AF19	C303 1uF	1 2 C0201 X5R 4V
MIPI_D/C_PHY1_VDD	AG19	C284 1uF X5R 6.3V C0201	VDD_0V75_S0
MIPI_D/C_PHY1_VDD_1V2	AH19	C280 100nF X5R 6.3V C0201	VDDA_1V2_S0
MIPI_D/C_PHY1_VDD_1V8	AJ19	C269 1uF X5R 6.3V C0201	VCC_1V8_S0

RK3588

RK3588_P(MIPI_DPHY_CSI_RX_PHY)

U4P

MIPI DPHY CSI_RX Port0

MIPI V1.2/2.5Gbps

MIPI_CSI0_CLK0P/MIPI_CSI0_CLK0N	AJ33 / AJ34	MIPI_CSI0_RX_CLK0P / MIPI_CSI0_RX_CLK0N
MIPI_CSI0_D0P/MIPI_CSI0_D0N	AG33 / AG34	MIPI_CSI0_RX_D0P / MIPI_CSI0_RX_D0N
MIPI_CSI0_D1P/MIPI_CSI0_D1N	AH33 / AH34	MIPI_CSI0_RX_D1P / MIPI_CSI0_RX_D1N
MIPI_CSI0_CLK1P/MIPI_CSI0_CLK1N	AM33 / AM34	
MIPI_CSI0_D2P/MIPI_CSI0_D2N	AK33 / AK34	MIPI_CSI0_RX_D2P / MIPI_CSI0_RX_D2N
MIPI_CSI0_D3P/MIPI_CSI0_D3N	AL33 / AL34	MIPI_CSI0_RX_D3P / MIPI_CSI0_RX_D3N
MIPI_CSI0_AVCC0V75	AB25	10mA VDD_0V75_S0
MIPI_CSI0_AVCC1V8	AB26	3.3mA VCC_1V8_S0

MIPI_CSI0_AVCC0V75: C343 100nF X5R 6.3V C0201; C363 1uF X5R 6.3V C0201
MIPI_CSI0_AVCC1V8: C346 1uF X5R 6.3V C0201

MIPI CSI Differential Pair:
100 Ohm +-10%

MIPI DPHY CSI_RX Port1

MIPI V1.2/2.5Gbps

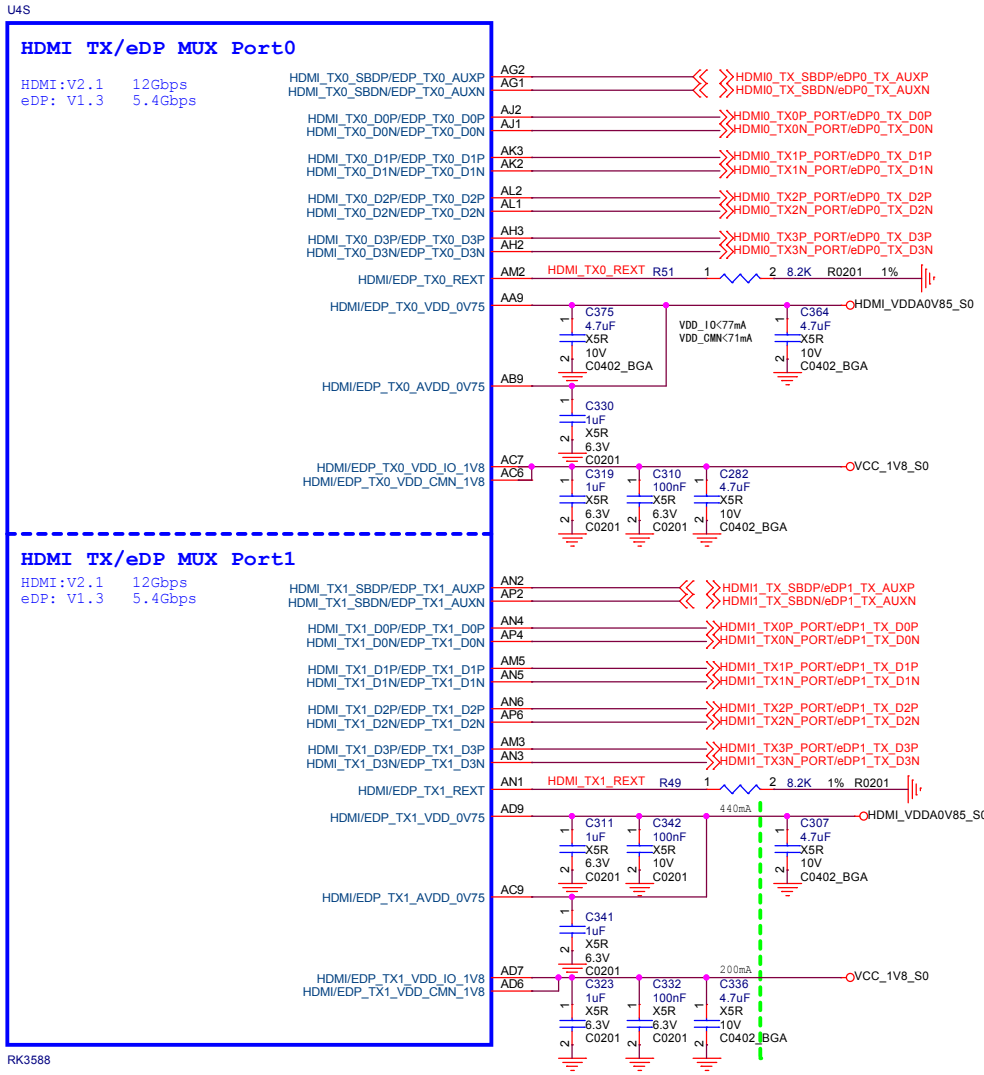
MIPI_CSI1_CLK0P/MIPI_CSI1_CLK0N	AJ31 / AJ32	MIPI_CSI1_RX_CLK0P / MIPI_CSI1_RX_CLK0N
MIPI_CSI1_D0P/MIPI_CSI1_D0N	AG31 / AG32	MIPI_CSI1_RX_D0P / MIPI_CSI1_RX_D0N
MIPI_CSI1_D1P/MIPI_CSI1_D1N	AH31 / AH32	MIPI_CSI1_RX_D1P / MIPI_CSI1_RX_D1N
MIPI_CSI1_CLK1P/MIPI_CSI1_CLK1N	AM31 / AM32	
MIPI_CSI1_D2P/MIPI_CSI1_D2N	AK31 / AK32	MIPI_CSI1_RX_D2P / MIPI_CSI1_RX_D2N
MIPI_CSI1_D3P/MIPI_CSI1_D3N	AL31 / AL32	MIPI_CSI1_RX_D3P / MIPI_CSI1_RX_D3N
MIPI_CSI1_AVCC0V75	AA25	VDD_0V75_S0
MIPI_CSI1_AVCC1V8	AA26	VCC_1V8_S0

MIPI_CSI1_AVCC0V75: C361 1uF X5R 6.3V C0201
MIPI_CSI1_AVCC1V8: C385 100nF X5R 6.3V C0201

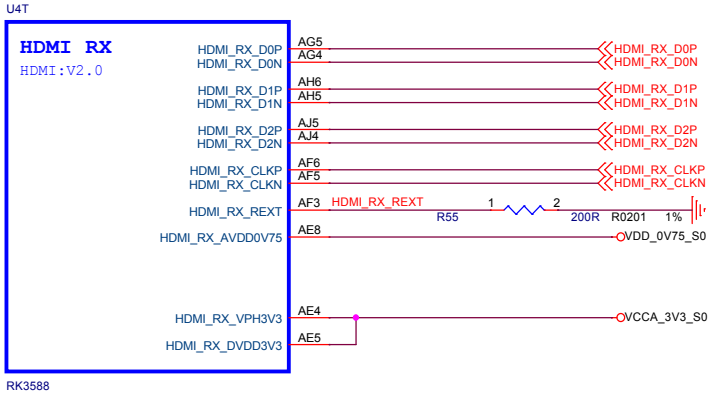
RK3588

Shenzhen Xunlong Software Co., Ltd					
Project:	OPi 5 Ultra				
File:	16.RK3588_MIPI Interface				
Date:	Monday, January 13, 2025			Rev:	V1.0
Size:	A3	Sheet:	7	Of:	28

RK3588_S(HDMI2.1 TX)

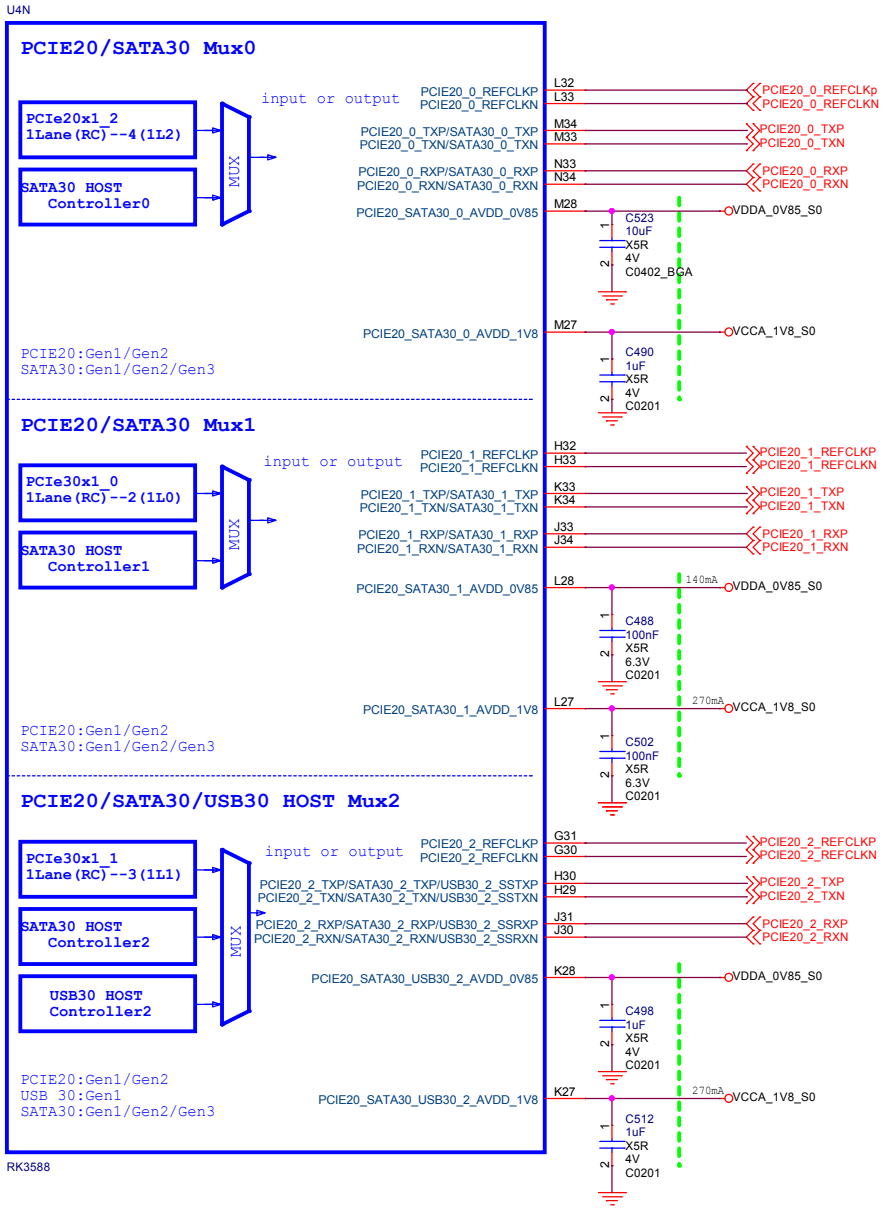


RK3588_T(HDMI20 RX)

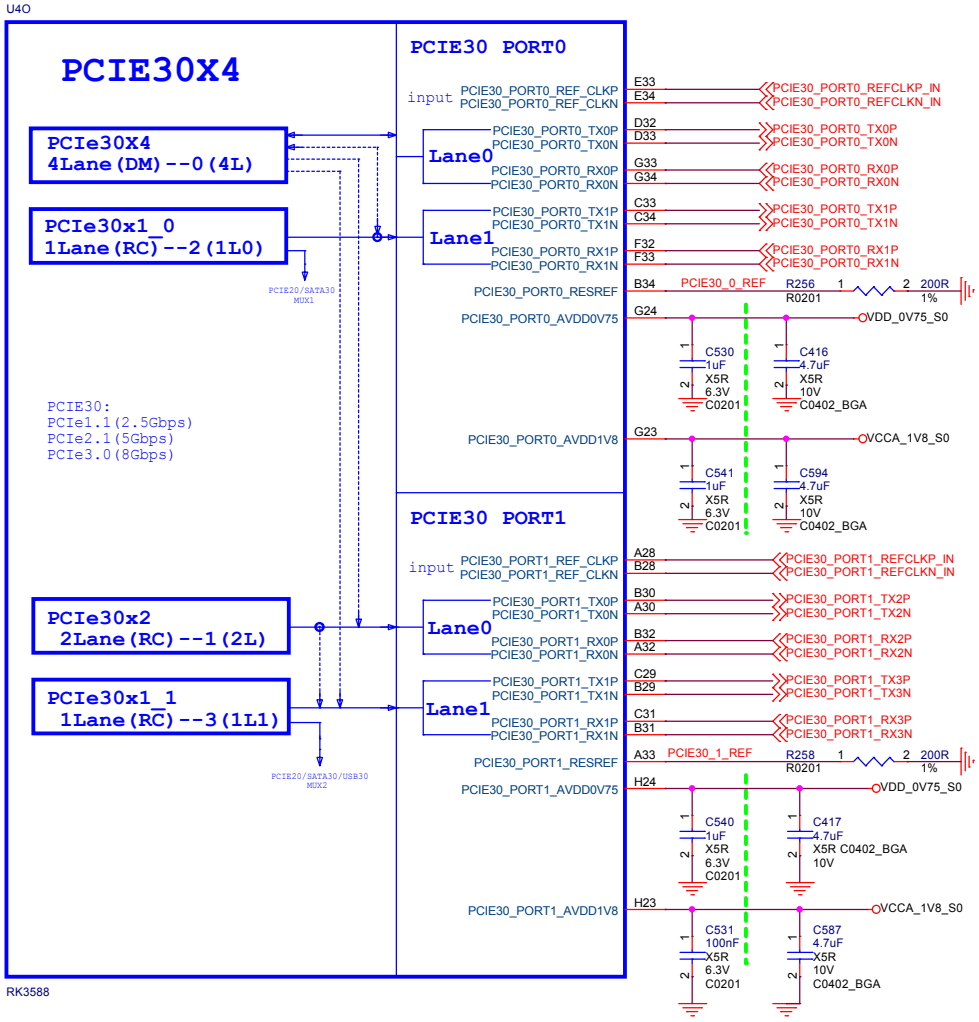


Shenzhen Xunlong Software Co., Ltd					
Project:	OPi 5 Ultra				
File:	17.RK3588_HDMI/eDP Interface				
Date:	Monday, January 13, 2025			Rev:	V1.0
Size:	A3	Sheet:	8	Of:	28

RK3588_N(PCIE20)



RK3588_O(PCIE30)



Shenzhen Xunlong Software Co., Ltd					
Project:	OPi 5 Ultra				
File:	18.RK3588_PCIE30/PCIE20/SATA30				
Date:	Monday, January 13, 2025			Rev:	V1.0
Size:	A3	Sheet:	9	Of:	28

RK3588_J(VCCIO5 Domain)

U4J

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

PWM10_M0	SPI4_MISO_M1		I2C6_SDA_M4	FSPI_D0_M2	I2S3_MCLK	SDIO_D0_M1	GMAC1_TXD2	GPIO3_A0_u
AUDDSM_LN	SPI4_MOSI_M1	PWM11_IR_M0	I2C6_SCL_M4	FSPI_D1_M2	I2S3_SCLK	SDIO_D1_M1	GMAC1_TXD3	GPIO3_A1_u
AUDDSM_LP	SPI4_CLK_M1	UART8_TX_M1		FSPI_D2_M2	I2S3_LRCK	SDIO_D2_M1	GMAC1_RXD2	GPIO3_A2_u
AUDDSM_RN	SPI4_CS0_M1	UART8_RX_M1		FSPI_D3_M2	I2S3_SDO	SDIO_D3_M1	GMAC1_RXD3	GPIO3_A3_u
AUDDSM_RP	SPI4_CS1_M1	UART8_RTSN_M1			I2S3_SDI	SDIO_CMD_M1	GMAC1_TXCLK	GPIO3_A4_d
	MIPI_CAMERA0_CLK_M1	UART8_CTSN_M1	I2C4_SDA_M0	FSPI_CLK_M2		SDIO_CLK_M1	GMAC1_RXCLK	GPIO3_A5_d
	MIPI_CAMERA1_CLK_M1		I2C4_SCL_M0				ETH1_REFCLKO_25M	GPIO3_A6_d
PWM8_M0	MIPI_CAMERA2_CLK_M1						GMAC1_RXD0	GPIO3_A7_u
PWM9_M0	MIPI_CAMERA3_CLK_M1						GMAC1_RXD1	GPIO3_B0_u
PWM2_M1	MIPI_CAMERA4_CLK_M1	UART2_TX_M2					GMAC1_RXDV_CRS	GPIO3_B1_d
PWM3_IR_M1		UART2_RX_M2			I2S2_SDI_M1		GMAC1_TXER	GPIO3_B2_d
		UART2_RTSN			I2S2_SDO_M1		GMAC1_TXD0	GPIO3_B3_u
		UART2_CTSN			I2S2_MCLK_M1		GMAC1_TXD1	GPIO3_B4_u
PWM12_M0	CAN1_RX_M0	UART3_TX_M1			I2S2_SCLK_M1		GMAC1_TXEN	GPIO3_B5_u
PWM13_M0	CAN1_TX_M0	UART3_RX_M1			I2S2_LRCK_M1		GMAC1_MCLKINOUT	GPIO3_B6_d
			I2C3_SCL_M1	SPI1_MOSI_M1	HDMI_TX1_HPD_M1		GMAC1_PTP_REF_CLK	GPIO3_B7_d
		UART7_TX_M1	I2C3_SDA_M1	SPI1_MISO_M1			GMAC1_PPSTRIG	GPIO3_C0_d
	PCIE30X2_BUTTON_RSTN	UART7_RX_M1		SPI1_CLK_M1			GMAC1_PPSCLK	GPIO3_C1_d
PWM14_M0		UART7_RTSN_M1	I2C8_SCL_M4	SPI1_CS0_M1		MIPI_TE0	GMAC1_MDC	GPIO3_C2_d
PWM15_IR_M0		UART7_CTSN_M1	I2C8_SDA_M4	SPI1_CS1_M1		MIPI_TE1	GMAC1_MDIO	GPIO3_C3_d
CAN2_RX_M0	PCIE30X4_CLKREQN_M2	UART5_TX_M1	FSPI_CS0N_M2	SPI3_CS0_M3	HDMI_TX1_CEC_M2		CIF_D8	GPIO3_C4_u
CAN2_TX_M0	PCIE30X4_WAKEN_M2	UART5_RX_M1	FSPI_CS1N_M2	SPI3_CS1_M3	HDMI_TX1_SDA_M1		CIF_D9	GPIO3_C5_u
	PCIE30X4_PERSTN_M2			SPI3_MISO_M3	HDMI_TX1_SCL_M1		CIF_D10	GPIO3_C6_u
	PCIE20X1_2_CLKREQN_M0		I2C5_SCL_M0	SPI3_MOSI_M3	HDMI_TX0_SCL_M2		CIF_D11	GPIO3_C7_u
PWM8_M2	PCIE20X1_2_WAKEN_M0	UART4_RX_M1	I2C5_SDA_M0	SPI3_CLK_M3	HDMI_TX0_SDA_M2		CIF_D12	GPIO3_D0_u
PWM9_M2	PCIE20X1_2_PERSTN_M0	UART4_TX_M1		SPI0_MISO_M3	HDMI_RX_CEC_M1		CIF_D13	GPIO3_D1_d
	PCIE30X2_CLKREQN_M2	UART9_RTSN_M2	I2C7_SCL_M2	SPI0_MOSI_M3	HDMI_RX_SCL_M1		CIF_D14	GPIO3_D2_d
PWM10_M2	PCIE30X2_WAKEN_M2	UART9_CTSN_M2	I2C7_SDA_M2	SPI0_CLK_M3	HDMI_RX_SDA_M1		CIF_D15	GPIO3_D3_d
	PCIE30X2_PERSTN_M2	UART9_RX_M2		SPI0_CS0_M3	HDMI_RX_HPDOUT_M1	HDMI_TX0_HPD_M1	MCU_JTAG_TCK_M1	GPIO3_D4_d
PWM11_IR_M3	PCIE30X4_BUTTON_RSTN	UART9_TX_M2		SPI0_CS1_M3	DP1_HPDIN_M0		MCU_JTAG_TMS_M1	GPIO3_D5_d

AA29	FSPI_D0	GPIO3_A0_u
AA30	FSPI_D1	GPIO3_A1_u
AD27	FSPI_D2	GPIO3_A2_u
AE27	FSPI_D3	GPIO3_A3_u
AD28	X	GPIO3_A4_d
AH30	FSPI_CLK	GPIO3_A5_d
AH27	CAM0_CLK	GPIO3_A6_d
AG29	CAM1_CLK	GPIO3_A7_u
AG28	CAM2_CLK	GPIO3_B0_u
AH29	CAM1_RST	GPIO3_B1_d
AE28	CAM2_RST	GPIO3_B2_d
AC28	CAM1_PDN	GPIO3_B3_u
AC29	CAM2_PDN	GPIO3_B4_u
AD29	GPIO3_B5	GPIO3_B5_u
AE29	GPIO3_B6	GPIO3_B6_d
AA28	GPIO3_B7	GPIO3_B7_d
Y29	GPIO3_C0	GPIO3_C0_d
Y27	GPIO3_C1	GPIO3_C1_d
Y31	GPIO3_C2	GPIO3_C2_d
Y30	MIPI_TE1	GPIO3_C3_d
AH26	FSPI_CS0	GPIO3_C4_u
AH25	HDMITX1_SDA_M1	GPIO3_C5_u
AG26	HDMITX1_SCL_M1	GPIO3_C6_u
AJ24	PCIE20_1_2_CLKREQn_M0_L	GPIO3_C7_u
AH24	PCIE20_1_2_WAKEn_M0_L	GPIO3_D0_u
AG23	FAN_CTL_H	GPIO3_D1_d
AG25	HP_DET_L	GPIO3_D2_d
AG24	HDMI_RX_DET_L	GPIO3_D3_d
AA27	PCIE20_1_2_PERSTN_L	GPIO3_D4_d
AB28	USB_HOST_PWREN	GPIO3_D5_d

VCCIO5_1V8 — W25 — C403 100nF X5R 6.3V C0201 — VCC_1V8_S0

VCCIO5 — W26 — C405 100nF X5R 6.3V C0201 — VCC_1V8_S0

RK3588

RK3588_K(VCCIO6 Domain)

U4K

VCCIO6 Domain

Operating Voltage=1.8V/3.3V

	SPI0_MISO_M1	UART9_RTSN_M1			I2S1_MCLK_M0	PCIE30X1_1_CLKREQN_M1	BT1120_D0	CIF_D0	GPIO4_A0_d
	SPI0_MOSI_M1	UART9_CTSN_M1			I2S1_SCLK_M0	PCIE30X1_1_WAKEN_M1	BT1120_D1	CIF_D1	GPIO4_A1_d
	SPI0_CLK_M1				I2S1_LRCK_M0	PCIE30X1_1_PERSTN_M1	BT1120_D2	CIF_D2	GPIO4_A2_d
		UART0_TX_M2				PCIE30X1_0_CLKREQN_M1	BT1120_D3	CIF_D3	GPIO4_A3_d
	SPI2_MISO_M1	UART0_RX_M2	I2C3_SCL_M2			PCIE30X1_0_WAKEN_M1	BT1120_D4	CIF_D4	GPIO4_A4_d
	SPI2_MOSI_M1	UART3_TX_M2	I2C3_SDA_M2		I2S1_SDI0_M0	PCIE30X1_0_PERSTN_M1	BT1120_D5	CIF_D5	GPIO4_A5_d
	SPI2_CLK_M1	UART3_RX_M2	I2C5_SCL_M2		I2S1_SDI1_M0	PCIE30X2_CLKREQN_M1	BT1120_D6	CIF_D6	GPIO4_A6_d
	SPI2_CS0_M1		I2C5_SDA_M2		I2S1_SDI2_M0	PCIE30X2_WAKEN_M1	BT1120_D7	CIF_D7	GPIO4_A7_d
	SPI2_CS1_M1	UART8_TX_M0	I2C6_SDA_M3		I2S1_SDI3_M0	PCIE30X2_PERSTN_M1	BT1120_CLKOUT	CIF_CLKIN	GPIO4_B0_d
SATA2_ACT_LED_M0	SPDIF1_TX_M1	SPI0_CS1_M1	UART8_RX_M0	I2C6_SCL_M3		I2S1_SDO0_M0	PCIE30X1_0_BUTTON_RSTN		MIPI_CAMERA5_CLK_M0	GPIO4_B1_u
CAN1_RX_M1	PWM14_M1	SPI0_CS0_M1	UART8_RTSN_M0	I2C7_SCL_M3		I2S1_SDO1_M0	PCIE30X1_1_BUTTON_RSTN	BT1120_D8	CIF_HREF	GPIO4_B2_u
CAN1_TX_M1	PWM15_IR_M1		UART8_CTSN_M0	I2C7_SDA_M3		I2S1_SDO2_M0	PCIE20X1_2_BUTTON_RSTN	BT1120_D9	CIF_VSYNC	GPIO4_B3_u
SPDIF0_TX_M1	PWM11_IR_M1	DP0_HPDIN_M0	UART9_TX_M1			I2S1_SDO3_M0	PCIE30X4_CLKREQN_M1	BT1120_D10	CIF_CLKOUT	GPIO4_B4_u
SATA1_ACT_LED_M0	PWM12_M1	SPI3_MISO_M1	UART9_RX_M1			HDMI_RX_CEC_M0	PCIE30X4_WAKEN_M1	BT1120_D11		GPIO4_B5_d
SATA0_ACT_LED_M0	PWM13_M1	SPI3_MOSI_M1		I2C5_SCL_M1		HDMI_RX_HPDOUT_M0	PCIE30X4_PERSTN_M1	BT1120_D12		GPIO4_B6_d
		SPI3_CLK_M1		I2C5_SDA_M1		HDMI_TX0_SCL_M0	PCIE20X1_2_CLKREQN_M1	BT1120_D13		GPIO4_B7_u
		SPI3_CS0_M1		I2C8_SCL_M3		HDMI_TX0_SDA_M0	PCIE20X1_2_WAKEN_M1	BT1120_D14		GPIO4_C0_u
SPDIF1_TX_M2	PWM6_M1	SPI3_CS1_M1		I2C8_SDA_M3		HDMI_TX0_CEC_M0	PCIE20X1_2_PERSTN_M1	BT1120_D15		GPIO4_C1_d

AK30	PCIE30x1_1_CLKREQn_M1_L	GPIO4_A0_d
AL30	PCIE30x1_1_WAKEn_M1_L	GPIO4_A1_d
AM29	PCIE30x1_1_PERSTn_M1_L	GPIO4_A2_d
AL29	PCIE30x1_0_CLKREQn_M1_L	GPIO4_A3_d
AL28	PCIE30x1_0_WAKEn_M1_L	GPIO4_A4_d
AK27	PCIE30x1_0_PERSTn_M1_L	GPIO4_A5_d
AL27	GPIO4_A6	GPIO4_A6_d
AM27	GPIO4_A7	GPIO4_A7_d
AK26	PHONE_CTL	GPIO4_B0_d
AL24	USB_OTG_PWREN	GPIO4_B1_u
AK25	HDMI1_TX_ON_H	GPIO4_B2_u
AM25	GPIO4_B3	GPIO4_B3_u
AL26	PCIE30X4_CLKREQn_M1_L	GPIO4_B4_u
AJ26	PCIE30X4_WAKEn_M1_L	GPIO4_B5_d
AJ27	PCIE30X4_PERSTn_M1_L	GPIO4_B6_d
AJ28	GPIO4_B7	GPIO4_B7_u
AJ25	GPIO4_C0	GPIO4_C0_u
AK24	GPIO4_C1	GPIO4_C1_d

VCCIO6_1V8 — AC25 — C327 100nF X5R 6.3V C0201 — VCC_1V8_S0

VCCIO6 — AC26 — C326 100nF X5R 6.3V C0201 — VCC_3V3_S0

RK3588

RK3588_I(VCCIO4 Domain)

U4I

VCCIO4 Domain

Operating Voltage=1.8V/3.3V

		SPI4_MISO_M2	PCIE30X1_1_CLKREQN_M2	DP0_HPDIN_M2		I2C2_SDA_M4	UART6_RX_M1	GPIO1_A0_d
SATA1_ACT_LED_M1		SPI4_MOSI_M2	PCIE30X1_1_WAKEN_M2	DP1_HPDIN_M2		I2C2_SCL_M4	UART6_TX_M1	GPIO1_A1_d
	PWM0_M2	SPI4_CLK_M2		VOP_POST_EMPTY		I2C4_SDA_M3	UART6_RTSN_M1	GPIO1_A2_d
	PWM1_M2	SPI4_CS0_M2		HDMI_TX1_SDA_M2		I2C4_SCL_M3	UART6_CTSN_M1	GPIO1_A3_d
		SPI2_MISO_M0		HDMI_TX1_SCL_M2				GPIO1_A4_d
		SPI2_MOSI_M0		HDMI_TX0_HPD_M0				GPIO1_A5_d
		SPI2_CLK_M0		HDMI_TX1_HPD_M0				GPIO1_A6_d
	PWM3_IR_M3	SPI2_CS0_M0	PCIE30X1_1_PERSTN_M2			PDM1_SDI0_M1		GPIO1_A7_u
		SPI2_CS1_M0	PCIE30X4_CLKREQN_M3			PDM1_SDI1_M1		GPIO1_B0_u
		SPI0_MISO_M2	PCIE30X4_WAKEN_M3			PDM1_SDI2_M1		GPIO1_B1_d
		SPI0_MOSI_M2	PCIE30X4_PERSTN_M3			PDM1_SDI3_M1	UART4_RX_M2	GPIO1_B2_d
SATA0_ACT_LED_M1		SPI0_CLK_M2	PCIE30X1_0_WAKEN_M2			PDM1_CLK1_M1	UART4_TX_M2	GPIO1_B3_d
		SPI0_CS0_M2	PCIE30X1_0_PERSTN_M2			PDM1_CLK0_M1	UART7_RX_M2	GPIO1_B4_u
		SPI0_CS1_M2	PCIE30X1_0_CLKREQN_M2				UART7_TX_M2	GPIO1_B5_u
	HDMI_RX_HPDOUT_M2	SPDIF0_TX_M0	PCIE30X2_WAKEN_M3	MIPI_CAMERA1_CLK_M0		I2C5_SCL_M3	UART1_TX_M1	GPIO1_B6_u
SATA2_ACT_LED_M1	HDMI_RX_CEC_M2	PWM13_M2	SPDIF1_TX_M0	PCIE30X2_PERSTN_M3	MIPI_CAMERA2_CLK_M0		I2C5_SDA_M3	UART1_RX_M1	GPIO1_B7_u
	HDMI_RX_SCL_M2	PWM14_M2			MIPI_CAMERA3_CLK_M0		I2C8_SCL_M2	UART1_RTSN_M1	GPIO1_D6_u
	HDMI_RX_SDA_M2	PWM15_IR_M3		PCIE30X2_CLKREQN_M3	MIPI_CAMERA4_CLK_M0		I2C8_SDA_M2	UART1_CTSN_M1	GPIO1_D7_u

A24	GPIO1_A0	GPIO1_A0_d
A25	GPIO1_A1	GPIO1_A1_d
A26	GPIO1_A2	GPIO1_A2_d
A27	GPIO1_A3	GPIO1_A3_d
B25	GPIO1_A4	GPIO1_A4_d
B26	HDMITX0_HPDIN_M0	GPIO1_A5_d
C24	HDMITX1_HPDIN_M0	GPIO1_A6_d
C25	GPIO1_A7/PWM3_IR_M3	GPIO1_A7_u
C27	GPIO1_B0	GPIO1_B0_u
D25	GPIO1_B1	GPIO1_B1_d
D26	GPIO1_B2	GPIO1_B2_d
D27	GPIO1_B3	GPIO1_B3_d
E24	GPIO1_B4	GPIO1_B4_u
E25	GPIO1_B5	GPIO1_B5_u
E26	HDMII_RX_HPDOUT_M2	GPIO1_B6_u
E27	HDMI_RX_CEC_M2	GPIO1_B7_u
F24	HDMI_RX_SCL_M2	GPIO1_D6_u
F25	HDMI_RX_SDA_M2	GPIO1_D7_u

VCCIO4_1V8 — H20 — C543 100nF X5R 6.3V C0201 — VCC_1V8_S0

VCCIO4 — H21 — C534 100nF X5R 6.3V C0201 — VCC_3V3_S0

RK3588

Shenzhen Xunlong Software Co., Ltd			
Project:	OPi 5 Ultra		
File:	19.RK3588_1.8V/ 3.3V GPIO		
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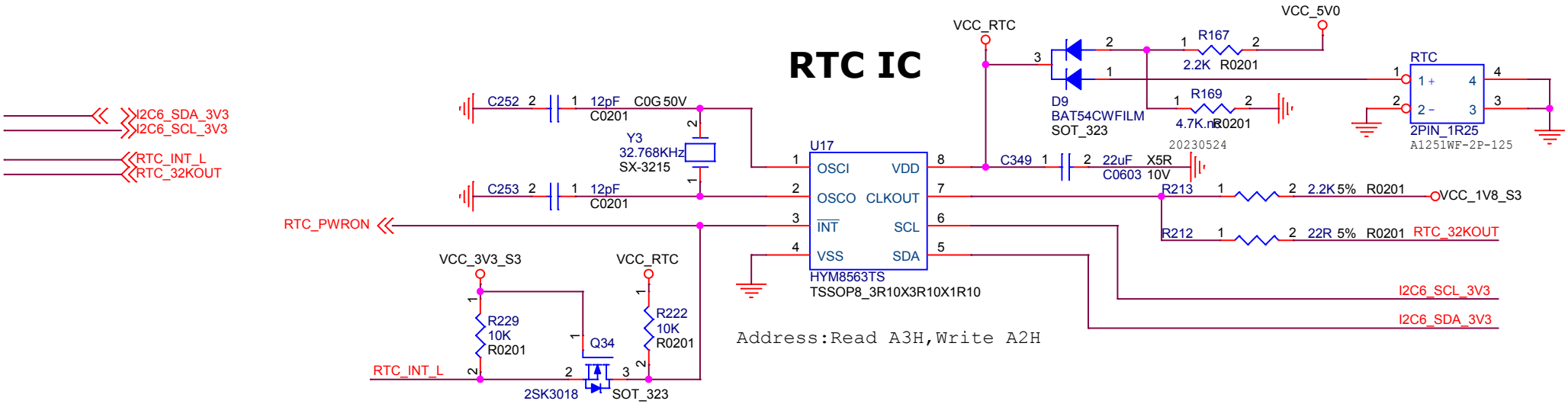
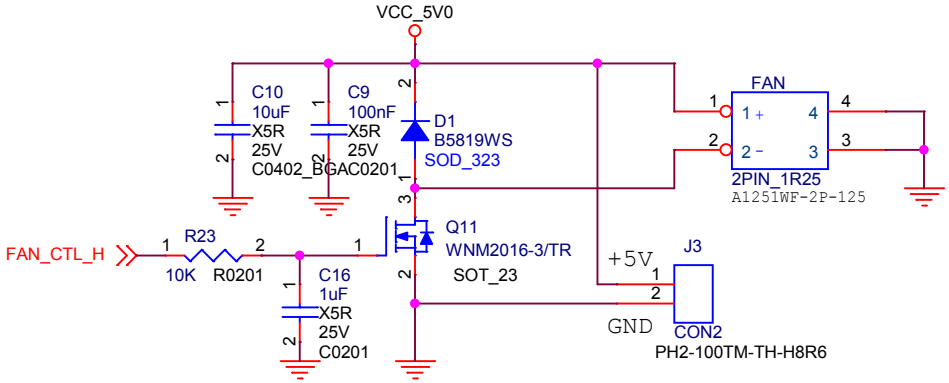
RTC IC

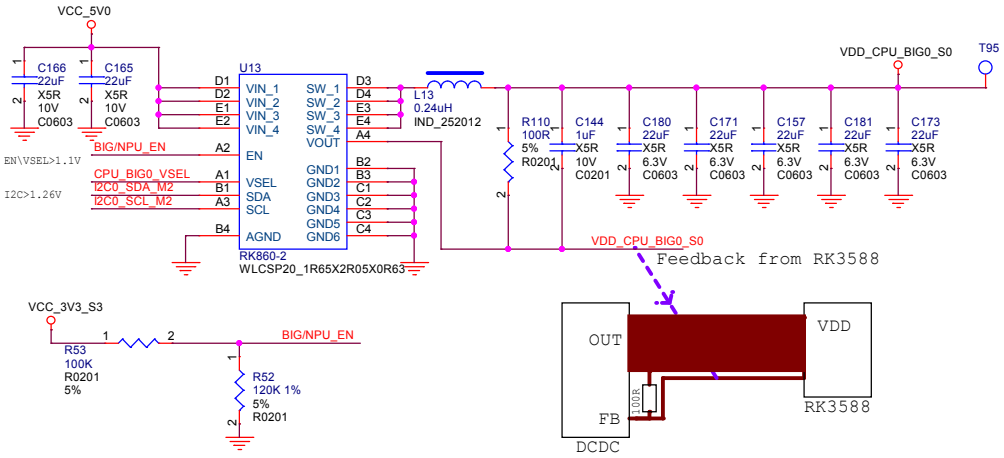


FAN_POWER

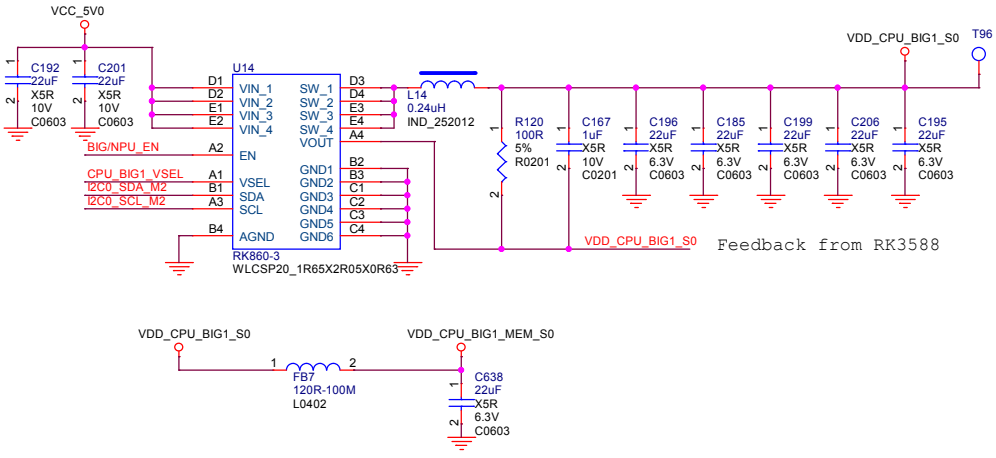


Shenzhen Xunlong Software Co., Ltd					
Project:	**OPi 5 Ultra**				
File:	**20.RTC/FAN**				
Date:	**Monday, January 13, 2025**			**Rev:**	**V1.0**
Size:	**A3**	**Sheet:**	**11**	**Of:**	**28**

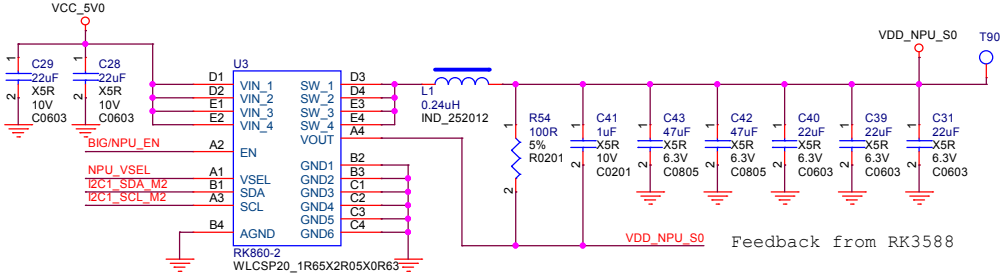
VDD_CPU_BIG0

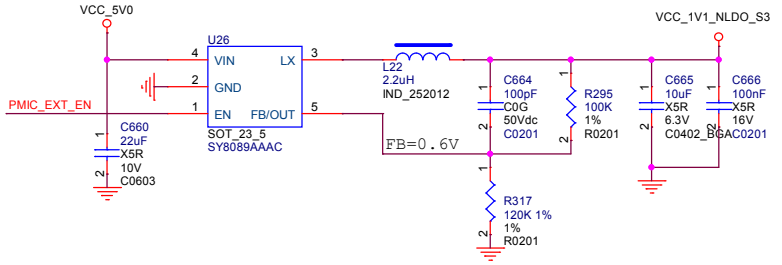


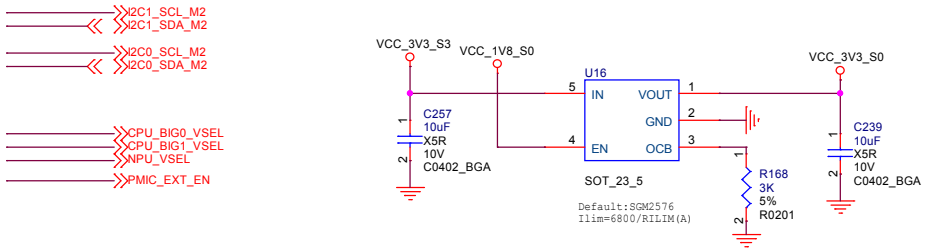
VDD_CPU_BIG1



VDD_NPU







Shenzhen Xunlong Software Co., Ltd					
Project:	OPi 5 Ultra				
File:	21.Power_Ext Discrete				
Date:	Monday, January 13, 2025			Rev:	V1.0
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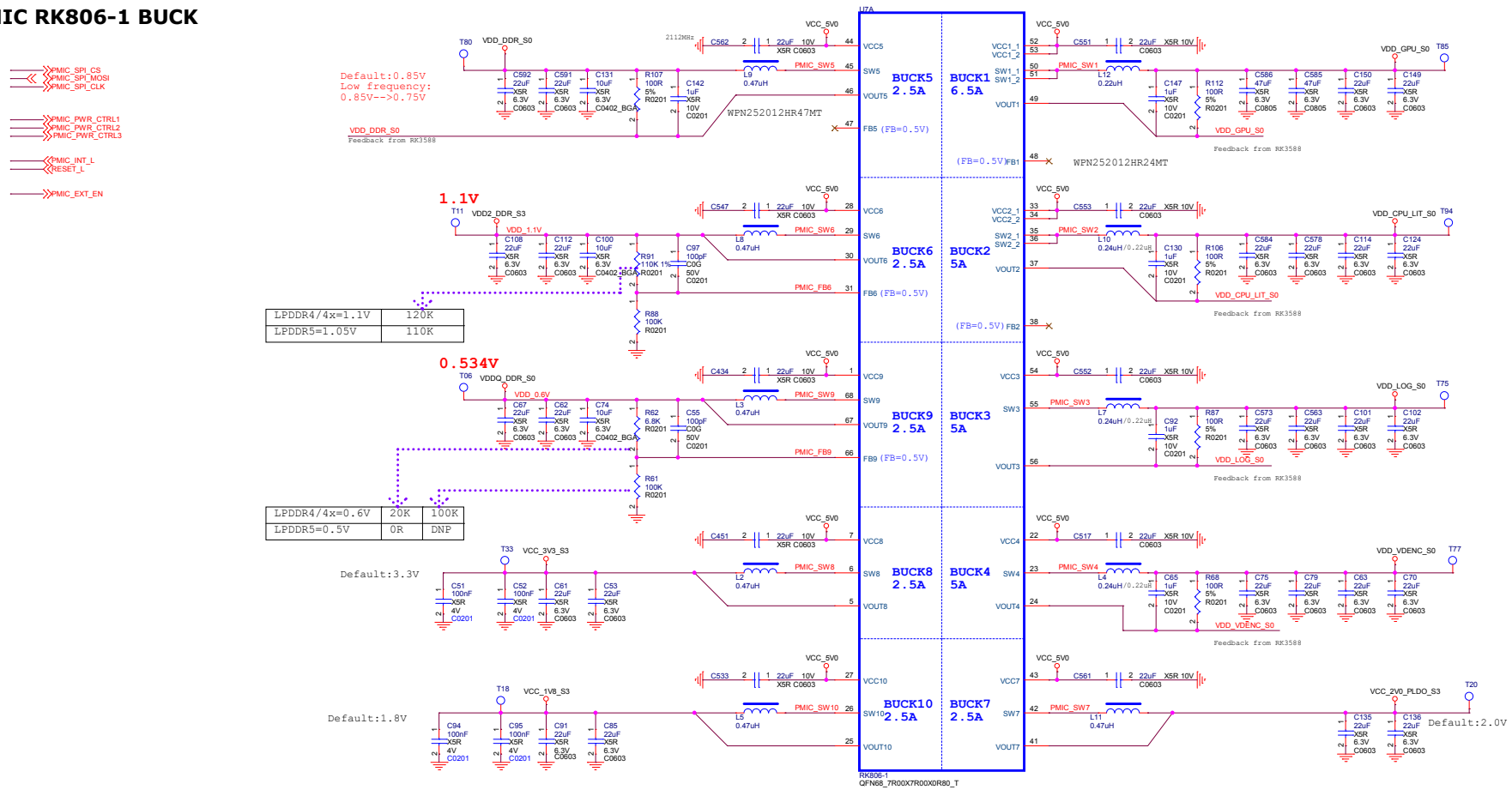
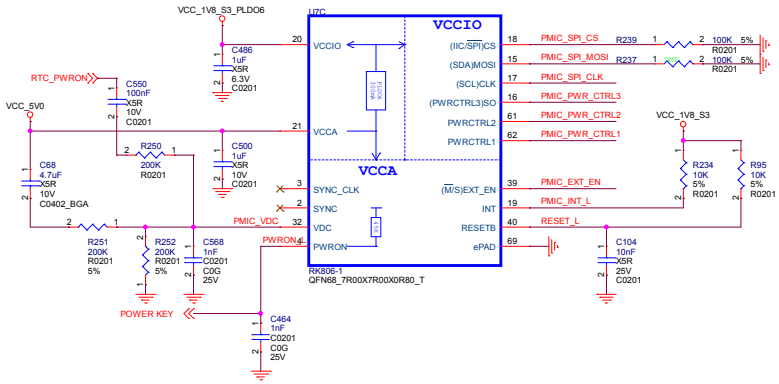
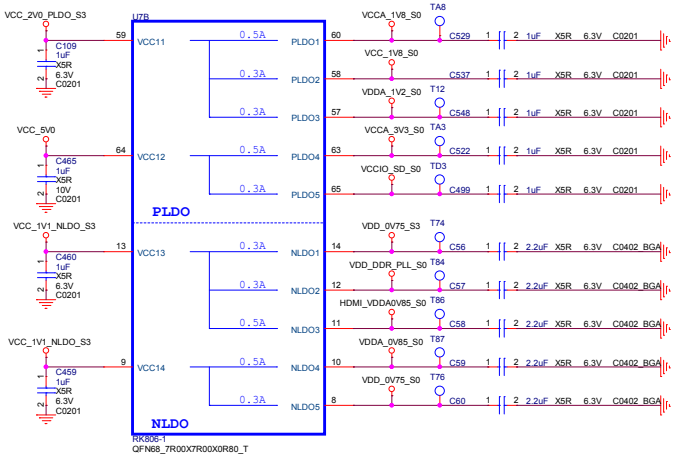
PMIC RK806-1 BUCK



PMIC RK806-1 Managerment



PMIC RK806-1 LDO



Shenzhen Xunlong Software Co., Ltd			
Project:	OPi 5 Ultra		
File:	22.Power-PMIC_RK806-1		
Date:	Monday, January 13, 2025	Rev:	V1.0
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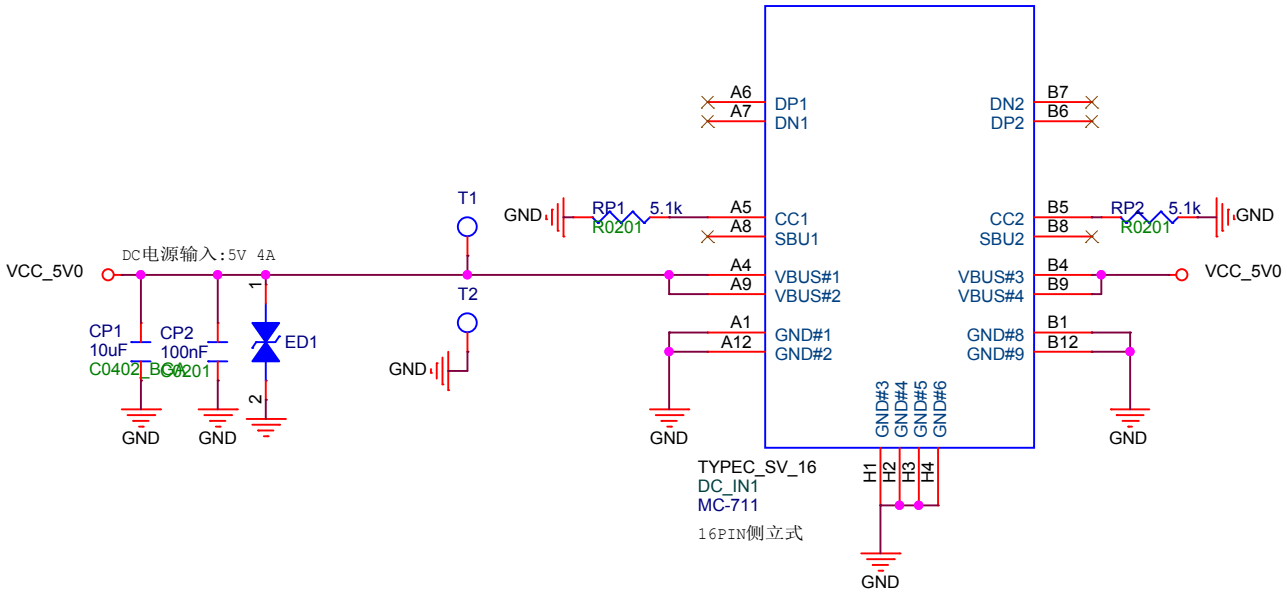
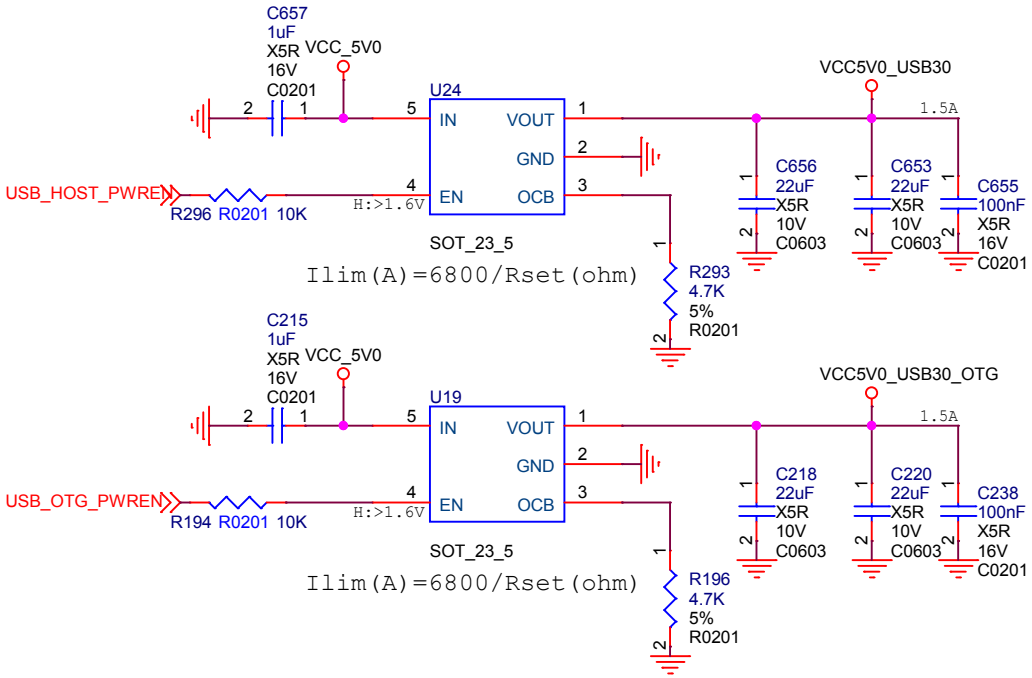
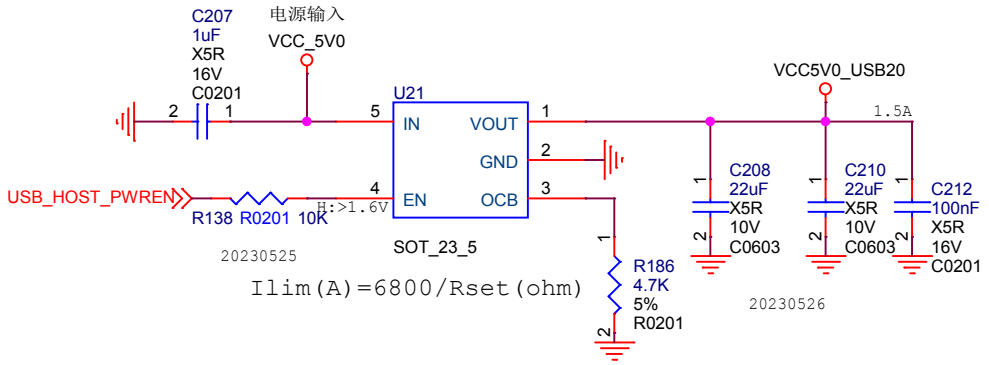
TPYE-C POWER IN

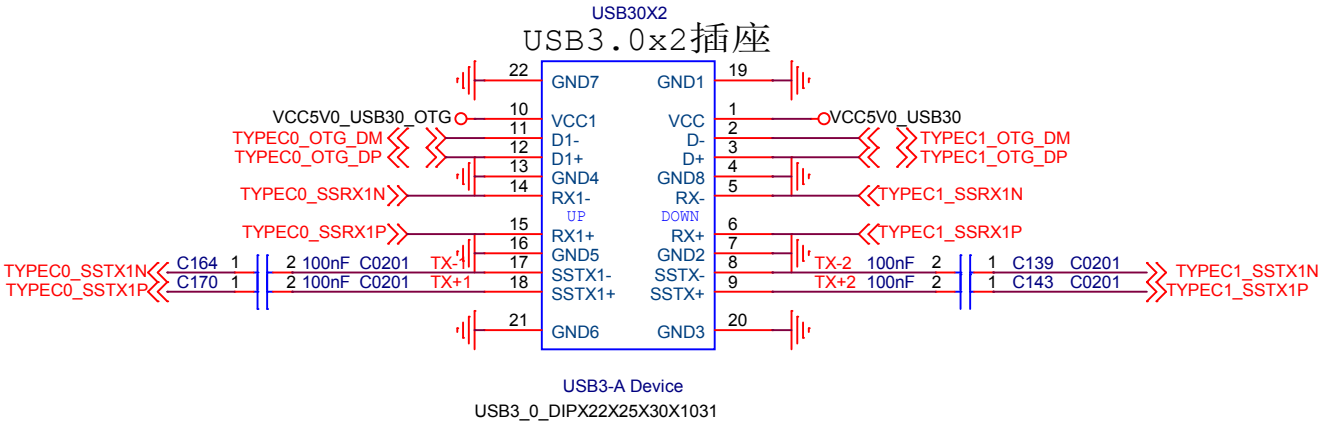


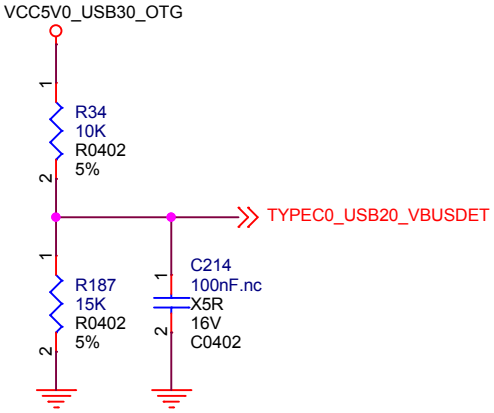
Shenzhen Xunlong Software Co., Ltd					
Project:	OPi 5 Ultra				
File:	23.Type C/DCIN				
Date:	Monday, January 13, 2025			Rev:	V1.0
Size:	A3	Sheet:	14	Of:	28



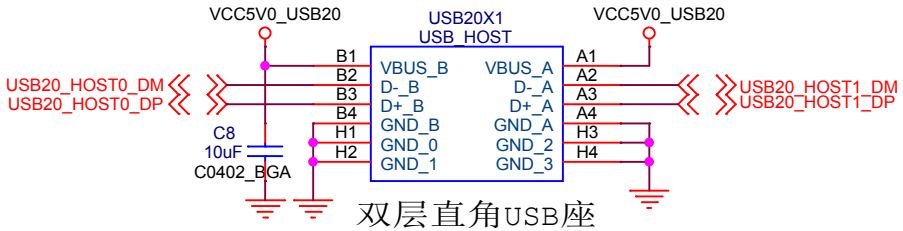


USB3.0*2





USB2.0*2



Shenzhen Xunlong Software Co., Ltd					
Project:	OPi 5 Ultra				
File:	24.USB30/USB20				
Date:	Monday, January 13, 2025			Rev:	V1.0
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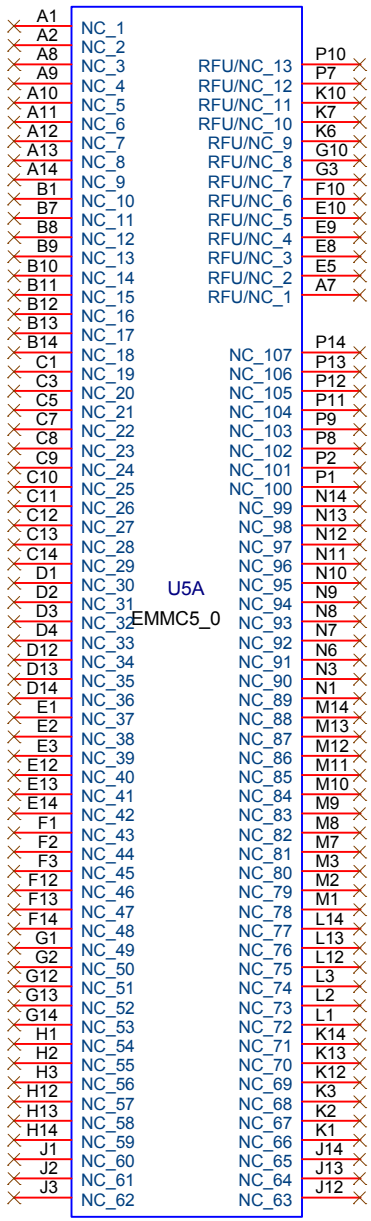
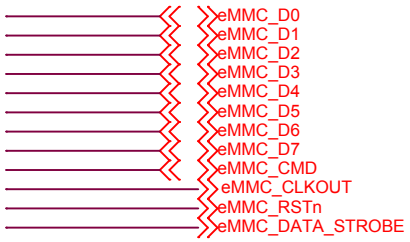
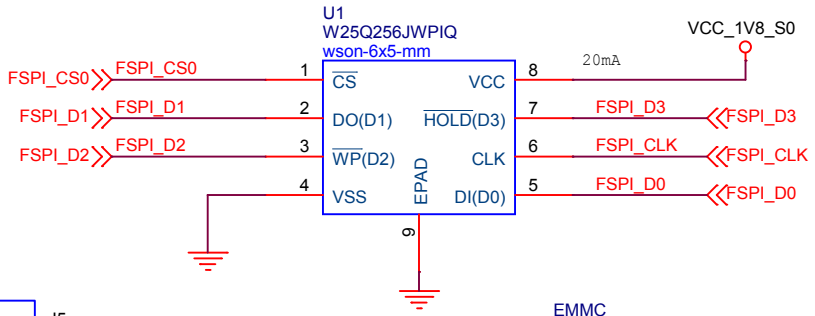
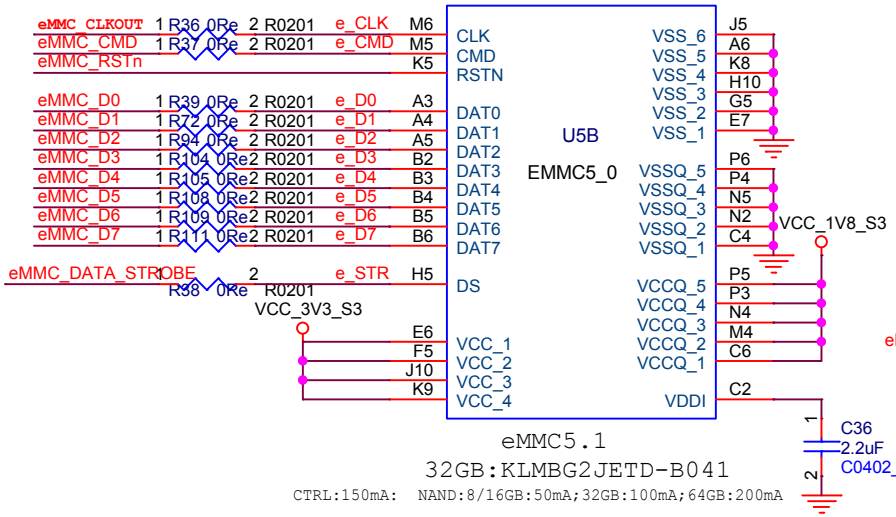
eMMC Flash

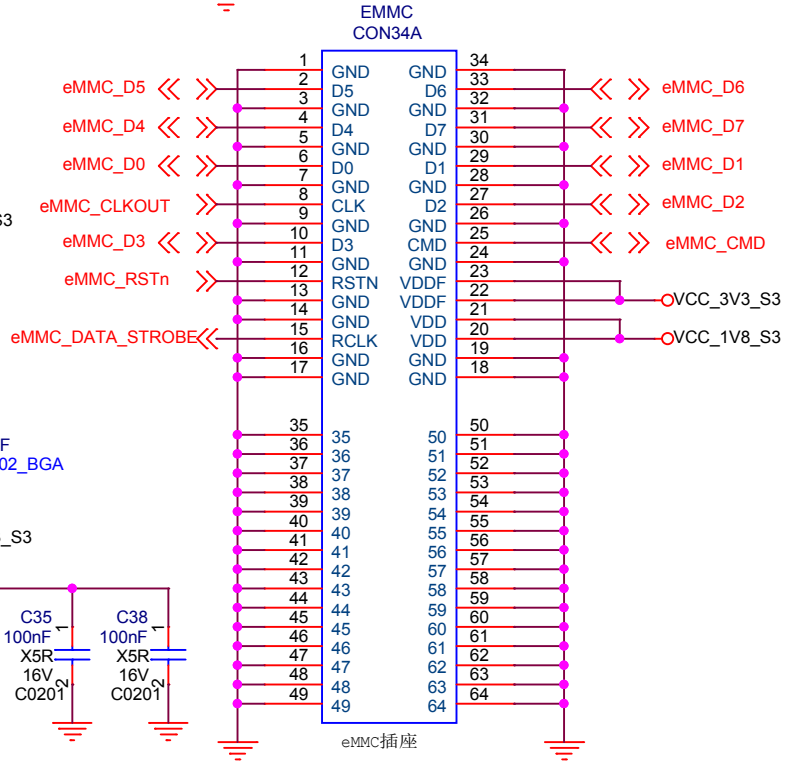


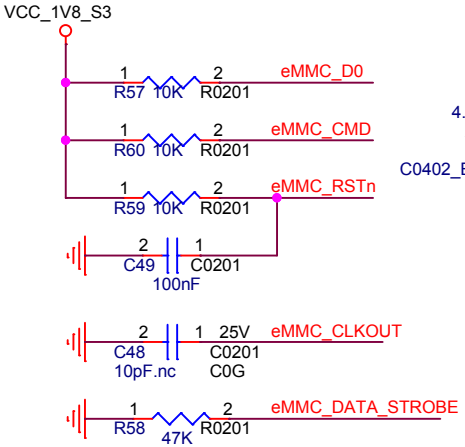


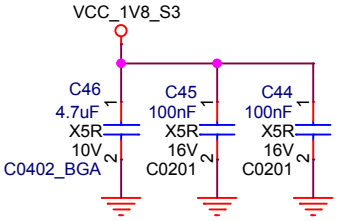
SPI FLASH:1.8V





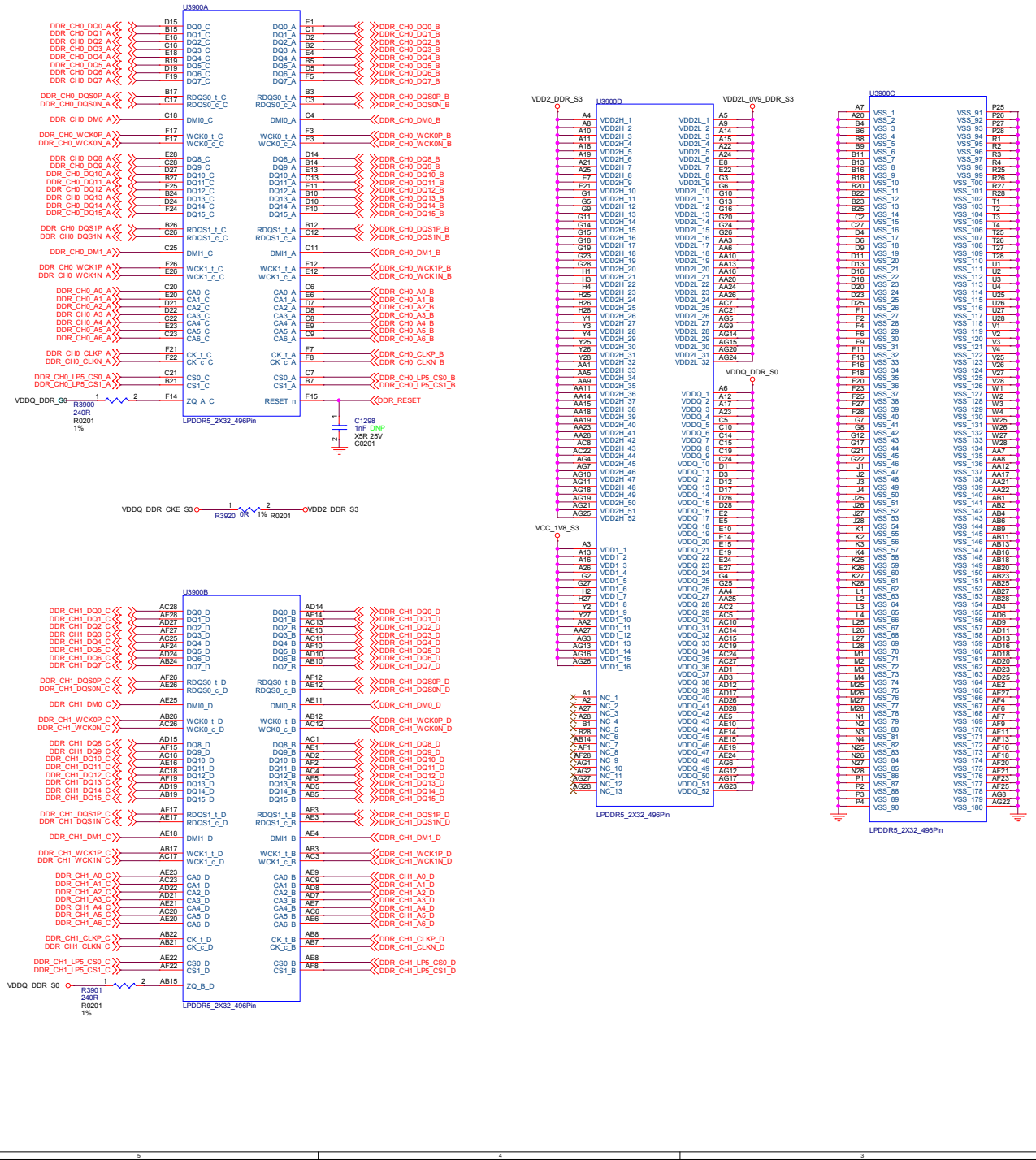






Shenzhen Xunlong Software Co., Ltd					
Project:	OPi 5 Ultra				
File:	25. eMMC/SPI Flash				
Date:	Monday, January 13, 2025			Rev:	V1.0
Size:	A3	Sheet:	16	Of:	28

DRAM-LPDDR5X_2X32bit

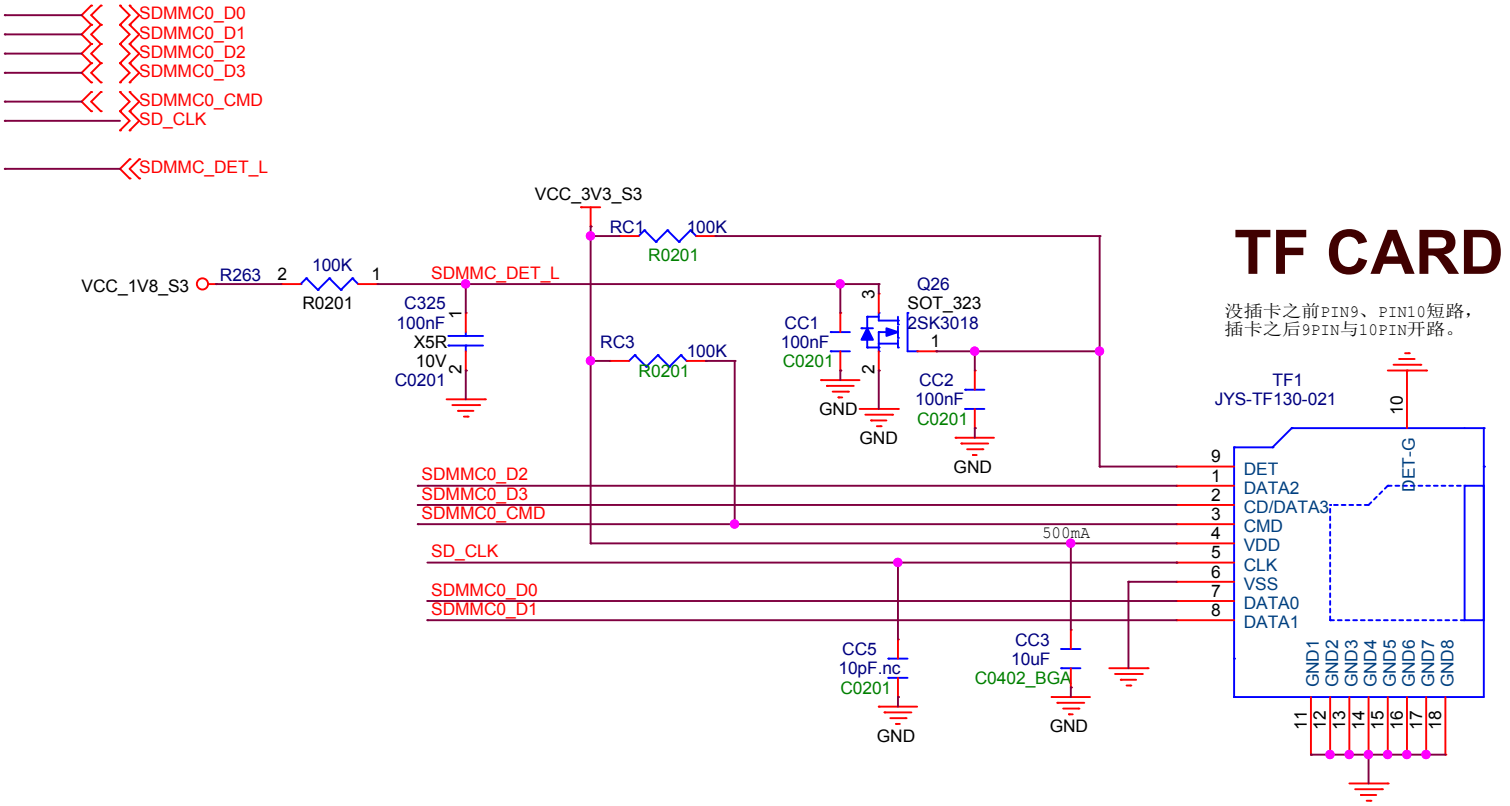


Power sequence: VDD1>VDD2H>=VDD2L>VDDQ-200mV

VDD1: 1.70V--1.95V
VDD2H:1.01V--1.12V
VDD2L:0.87V--0.97V
VDDQ: 0.47V--0.57V

Shenzhen Xunlong Software Co., Ltd				
Project:	OPi 5 Ultra			
File:	26.DRAM-LPDDR5X_496P_2X32bit			
Date:	Monday, January 13, 2025		Rev:	V1.0
Size:	A3	Sheet: 17	Of:	28

TF CARD

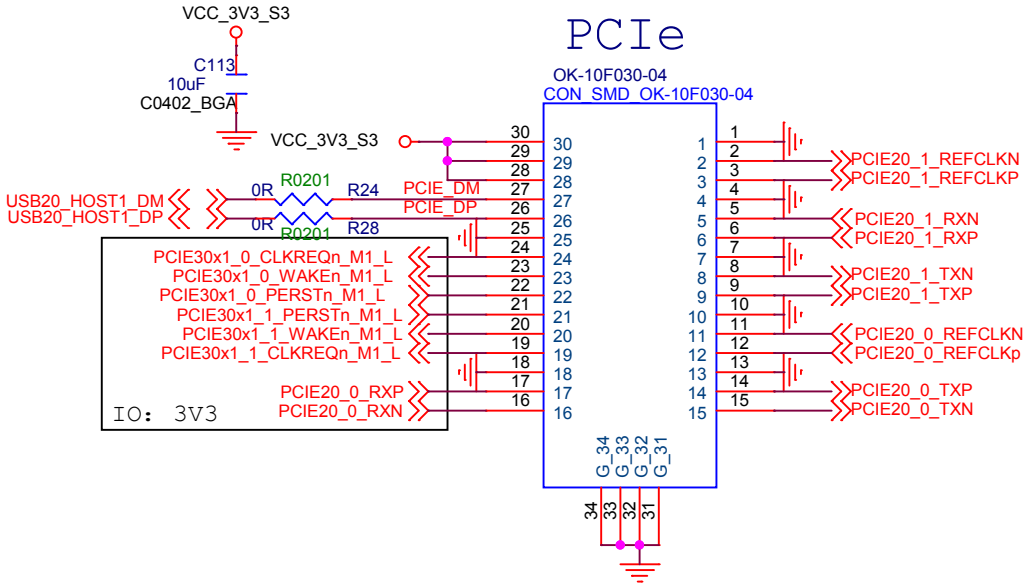


TF CARD

没插卡之前PIN9、PIN10短路，
插卡之后9PIN与10PIN开路。

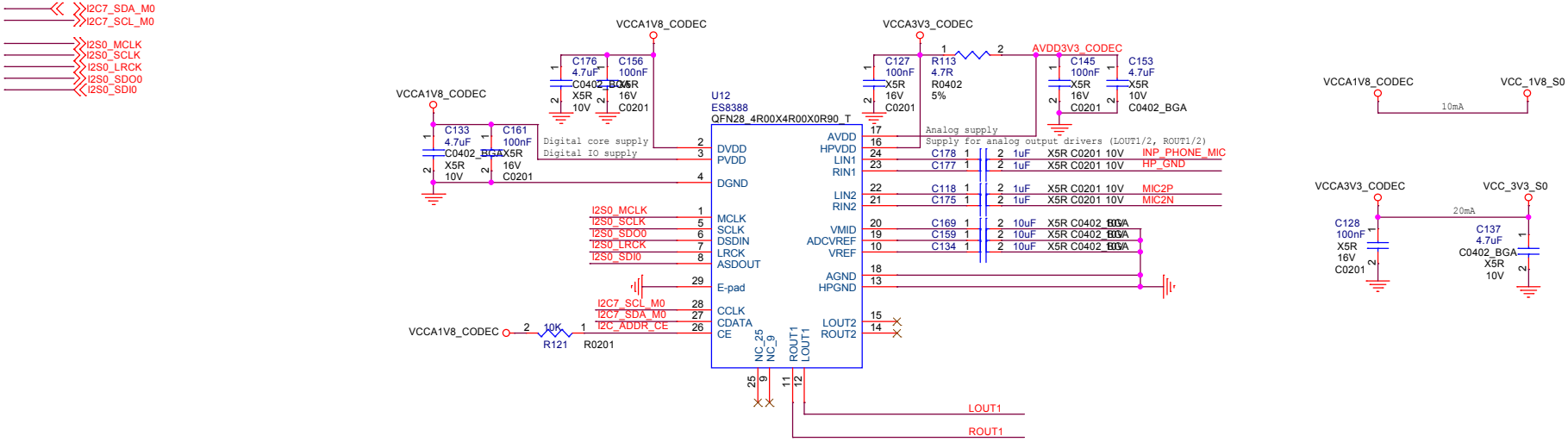
Rockchip Confidential

Shenzhen Xunlong Software Co., Ltd					
Project:	OPi 5 Ultra				
File:	27.Flash-TF Card				
Date:	Monday, January 13, 2025			Rev:	V1.0
Size:	A3	Sheet:	18	Of:	28

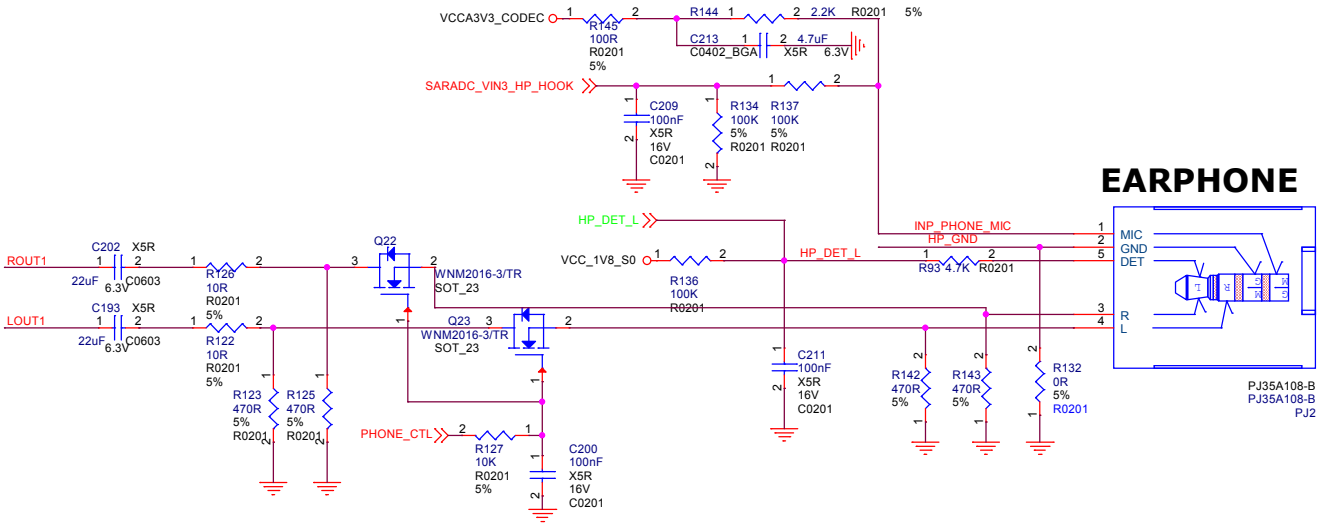


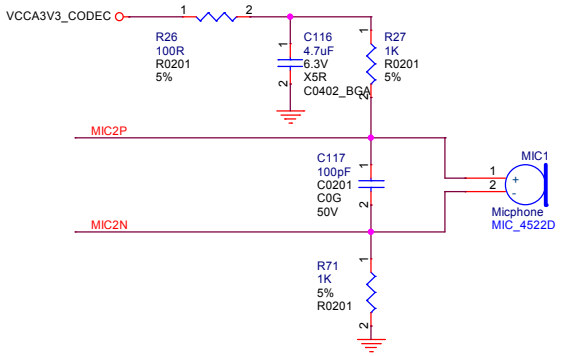
Shenzhen Xunlong Software Co., Ltd					
Project:	OPi 5 Ultra				
File:	28..EXT_30PIN_PCIe				
Date:	Monday, January 13, 2025			Rev:	V1.0
Size:	A3	Sheet:	19	Of:	28

CODEC ES8388



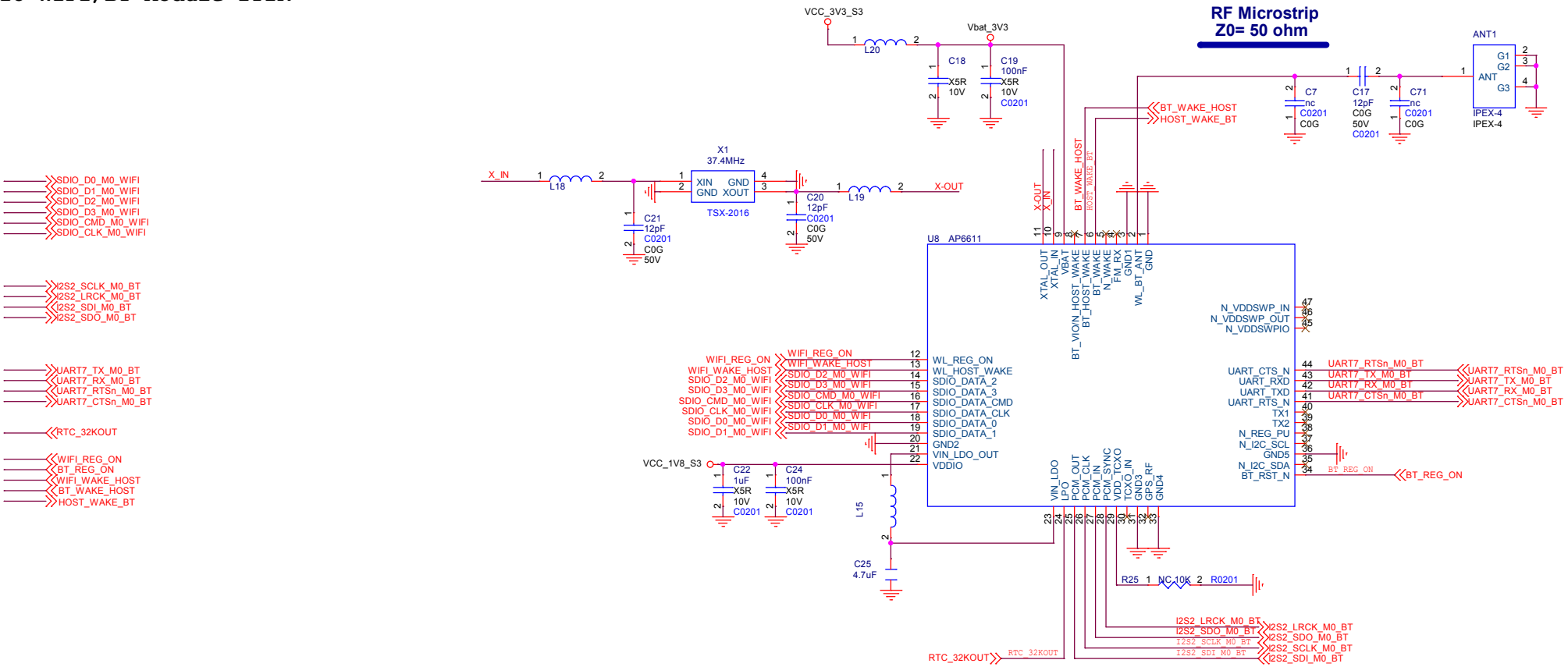
EARPHONE



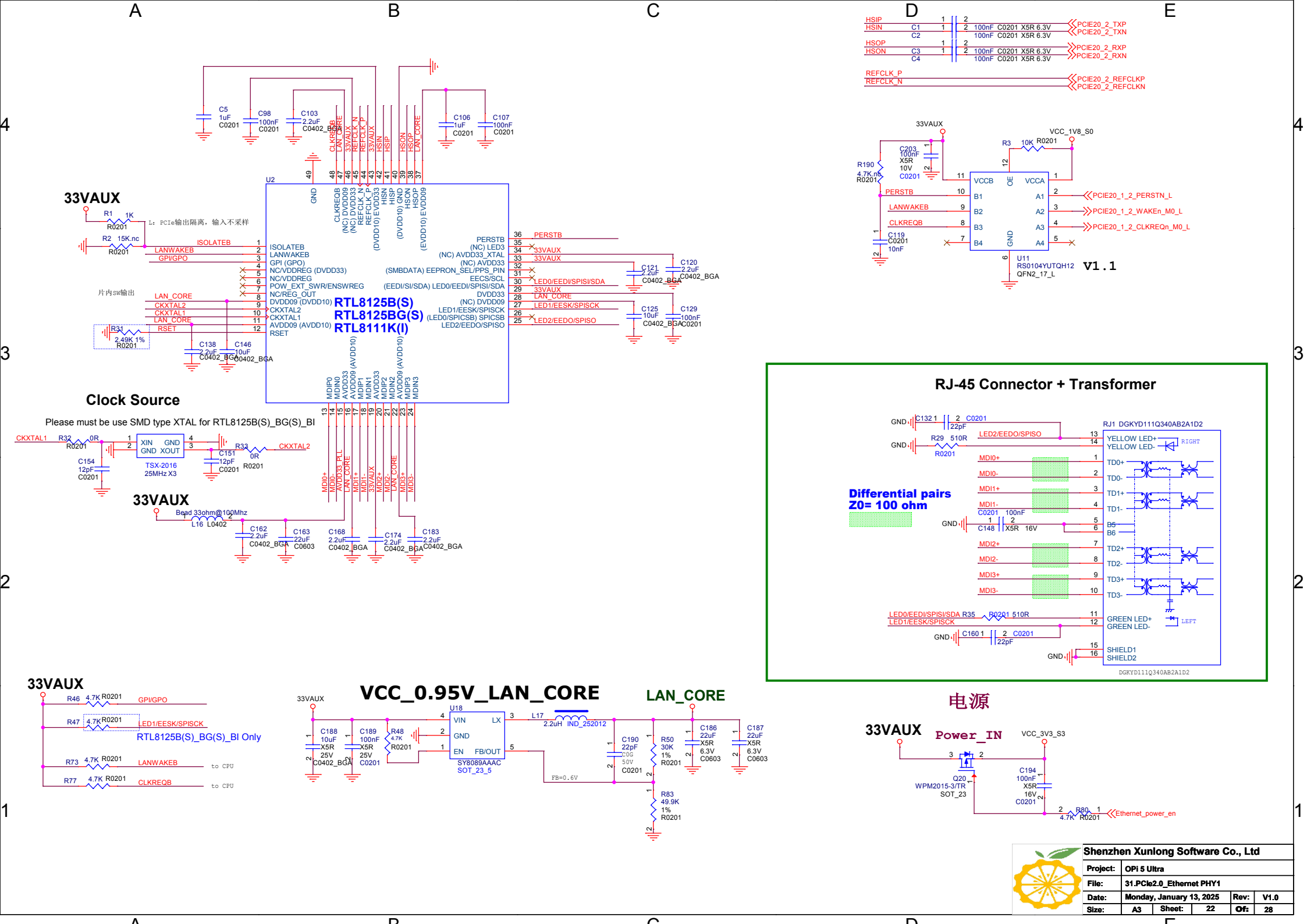


Shenzhen Xunlong Software Co., Ltd					
Project:	OPi 5 Ultra				
File:	29.Audio Codec				
Date:	Monday, January 13, 2025			Rev:	V1.0
Size:	A3	Sheet:	20	Of:	28

SDIO WIFI/BT Module-1T1R

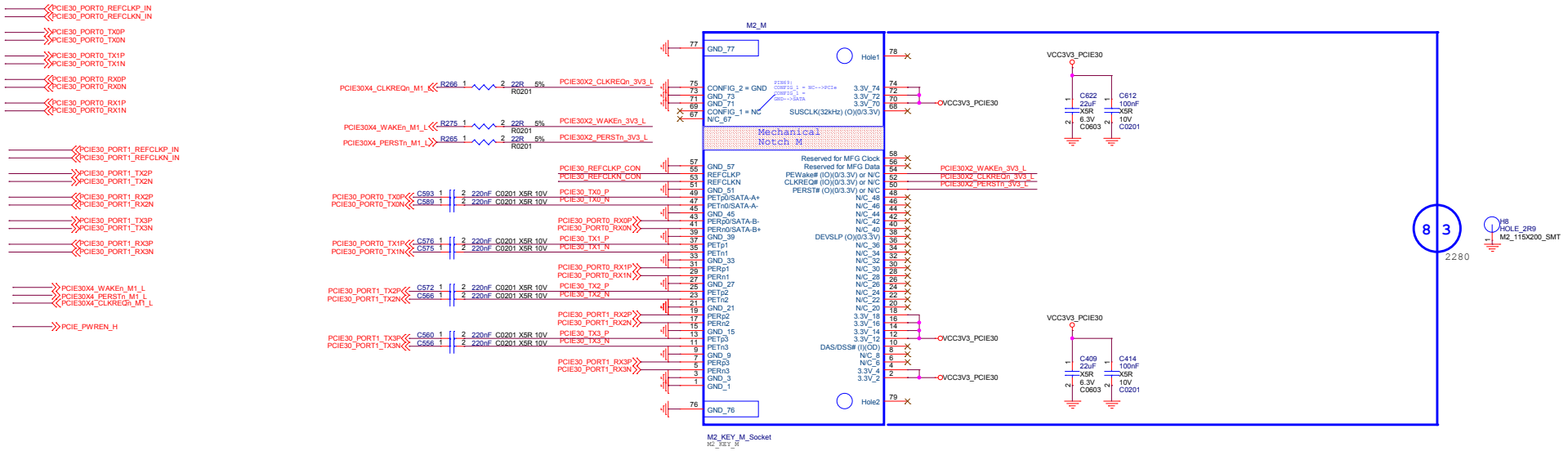


Shenzhen Xunlong Software Co., Ltd					
Project:	OPi 5 Ultra				
File:	30.WIFI/BT-SDIO_1T1R+UART				
Date:	Monday, January 13, 2025			Rev:	V1.0
Size:	A3	Sheet:	21	Of:	28

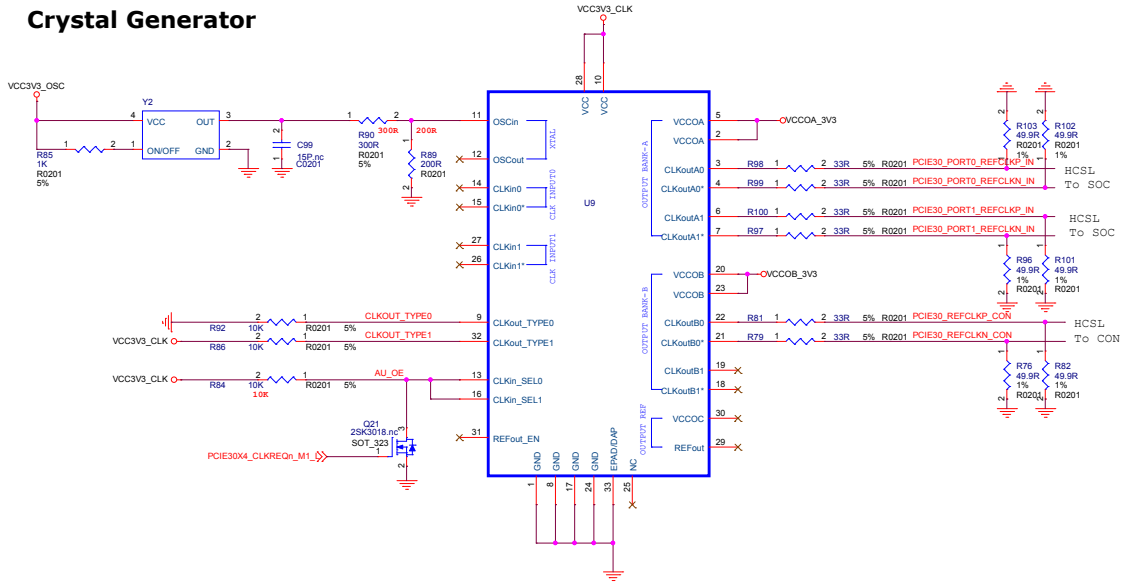


Shenzhen Xunlong Software Co., Ltd					
Project:	OPi 5 Ultra				
File:	31.PCIe2.0_Ethernet PHY1				
Date:	Monday, January 13, 2025		Rev:	V1.0	
Size:	A3	Sheet: 22	Of:	28	

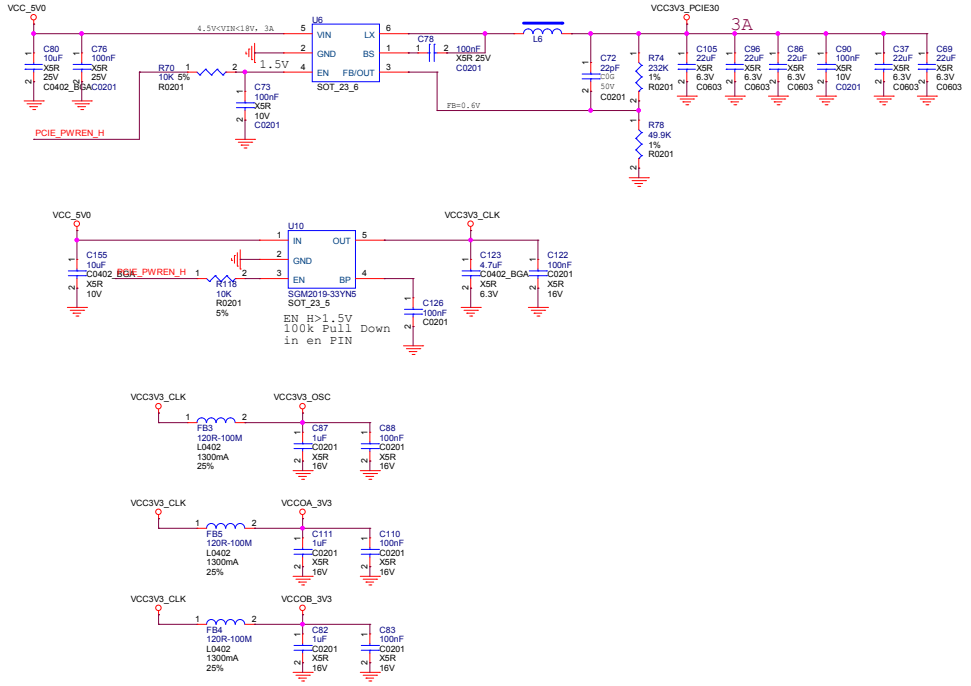
M.2_PCIe3.0 x 2Lanes



Crystal Generator



M.2 Power



Shenzhen Xunlong Software Co., Ltd			
Project:	OPi 5 Ultra		
File:	32.PCIe-M.2 _MKEY _PCIe3.0*4		
Date:	Monday, January 13, 2025	Rev:	V1.0
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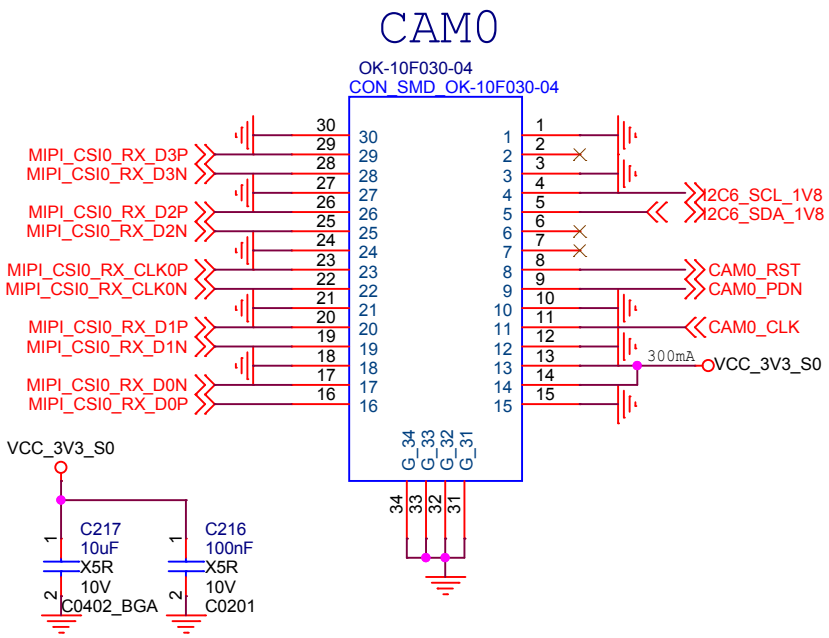
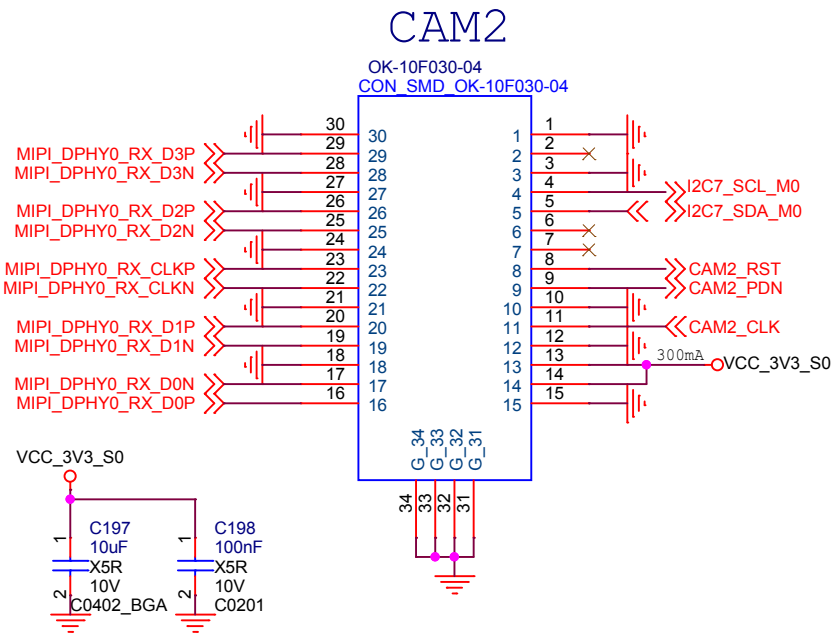
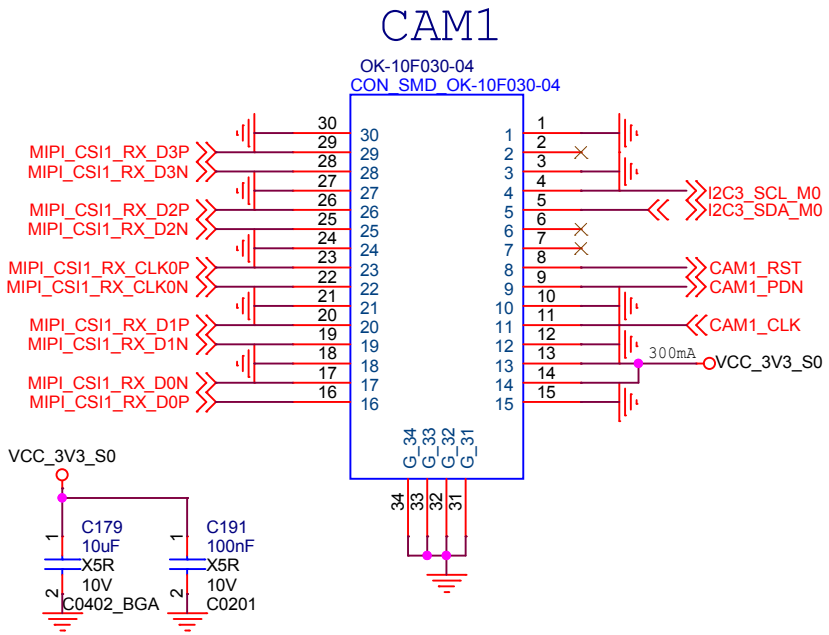
MIPI-CSI0_RX







Shenzhen Xunlong Software Co., Ltd					
Project:	OPi 5 Ultra				
File:	33.VI-Camera_MIPI_CSI-RX				
Date:	Monday, January 13, 2025			Rev:	V1.0
Size:	A3	Sheet:	24	Of:	28

HDMI TX1

HDMI1_TX_SBDP/eDP1_TX_AUXP
HDMI1_TX_SBDN/eDP1_TX_AUXN
HDMI1_TX0P_PORT/eDP1_TX_D0P
HDMI1_TX0N_PORT/eDP1_TX_D0N
HDMI1_TX1P_PORT/eDP1_TX_D1P
HDMI1_TX1N_PORT/eDP1_TX_D1N
HDMI1_TX2P_PORT/eDP1_TX_D2P
HDMI1_TX2N_PORT/eDP1_TX_D2N
HDMI1_TX3P_PORT/eDP1_TX_D3P
HDMI1_TX3N_PORT/eDP1_TX_D3N
HDMITX1_SDA_M1
HDMITX1_SCL_M1
HDMITX1_CEC_M0
HDMITX1_HPDIN_M0

VCC_5V0 — D8 B5819WS SOD_323 — VCC5V_HDMI_TX1

HDMI TX eARC

HDMI1_TX_SBDP/eDP1_TX_AUXP — C26 DNP / 1uF C0201 X5R 6.3V — HDMI1_TX_SBDP
HDMI1_TX_SBDN/eDP1_TX_AUXN — C27 1uF C0201 X5R 6.3V / DNP — HDMI1_TX_SBDN

VCC_3V3_S0
R43 47K R0201 5%
R42 47K R0201 5%
HDMITX1_HPDIN_M0
Q9 2SK3018 SOT_323
Q10 2SK3018 SOT_323
R44 47K R0201 5%
R45 1K R0201 5%
2.4-5.3V

HDMI TX DDC

VCC_5V0
VCC_1V8_S0
D5 B5819WS SOD_323
R5 2.2K 5% R0201
Q12 2SK3018 SOT_323
R6 2.2K 5% R0201
HDMITX1_SCL_M1 — HDMI1_TX_SCL_PORT
R8 2.2K 5% R0201
R9 1K 5% R0201
C12 100pF C0G 50V C0201
Q13 2SK3018 SOT_323
R7 2.2K 5% R0201
HDMITX1_SDA_M1 — HDMI1_TX_SDA_PORT

HDMI TX CEC

VCC_1V8_S0 VCC_5V0
R10 27K 5% R0201
Q14 2SK3018 SOT_323
HDMITX1_CEC_M0 — HDMI1_TX_CEC_PORT

HDMI1_TX2P_PORT/eDP1_TX_D2P — C222 / C223 — 220nF C0201 X5R 10V — HDMI1_TX2P_PORT
HDMI1_TX2N_PORT/eDP1_TX_D2N
HDMI1_TX1P_PORT/eDP1_TX_D1P — C226 / C227 — 220nF C0201 X5R 10V — HDMI1_TX1P_PORT
HDMI1_TX1N_PORT/eDP1_TX_D1N
HDMI1_TX0P_PORT/eDP1_TX_D0P — C230 / C231 — 220nF C0201 X5R 10V — HDMI1_TX0P_PORT
HDMI1_TX0N_PORT/eDP1_TX_D0N
HDMI1_TX3P_PORT/eDP1_TX_D3P — C234 / C235 — 220nF C0201 X5R 10V — HDMI1_TX3P_PORT
HDMI1_TX3N_PORT/eDP1_TX_D3N

HDMI1_TX2P_PORT
HDMI1_TX2N_PORT
HDMI1_TX1P_PORT
HDMI1_TX1N_PORT
HDMI1_TX0P_PORT
HDMI1_TX0N_PORT
HDMI1_TX3P_PORT
HDMI1_TX3N_PORT
HDMI1_TX_CEC_PORT
HDMI1_TX_SCL_PORT
HDMI1_TX_SDA_PORT
HDMI1_TX_SBDP
HDMI1_TX_SBDN
VCC5V_HDMI_TX1
C11 10uF X5R 10V C0402_BGA
J2 HDMI_TYPE_A hdmi-type-a

HDMI1_TX0P_PORT
HDMI1_TX0N_PORT
HDMI1_TX1P_PORT
HDMI1_TX1N_PORT
HDMI1_TX2P_PORT
HDMI1_TX2N_PORT
HDMI1_TX3P_PORT
HDMI1_TX3N_PORT
R166 590R 1% R0201
R165 590R 1% R0201
R154 590R 1% R0201
R153 590R 1% R0201
R158 590R 1% R0201
R157 590R 1% R0201
R162 590R 1% R0201
R161 590R 1% R0201
HDMI1_TX_ON_H
Q8 WNM6002-3/TR SOT_723
Q1 WNM6002-3/TR SOT_723
Q3 WNM6002-3/TR SOT_723
Q5 WNM6002-3/TR SOT_723
Rds=1.7ohm/2.6V
Coss=7.33pf

Note:
The controller only support AC coupled link In order to backward compatibility or to meet HDMI2.0 (1.4b) DC common mode spec and Voff, need do R based level-shift.

Switch on in HDMI2.0(TMDS) mode
Switch off in HDMI2.1(FRL) mode.

HDMI2.0 RX

HDMI_RX_D0P
HDMI_RX_D0N
HDMI_RX_D1P
HDMI_RX_D1N
HDMI_RX_D2P
HDMI_RX_D2N
HDMI_RX_CLKP
HDMI_RX_CLKN
HDMII_RX_HPDOUT_M2
HDMI_RX_CEC_M2
HDMI_RX_SCL_M2
HDMI_RX_SDA_M2
HDMI_RX_DET_L

HDMI RX DDC

VCC5V_HDMIRX_PORT
VCC_3V3_S0
D2 B5819WS SOD_323
R17 2.2K 5% R0201
Q6 2SK3018 SOT_323
R18 2.2K 5% R0201
HDMI_RX_SCL_M2 — HDMI_RXDDC_SCL_PORT
R151 2.2K 5% R0201
Q16 2SK3018 SOT_323
R152 2.2K 5% R0201
HDMI_RX_SDA_M2 — HDMI_RXDDC_SDA_PORT

VCC5V_HDMIRX_PORT
R15 100K R0201 5%
Q4 WPM3407-3/TR SOT_23
HDMI_RX_HPD_PORT
R14 1K R0201 5%
R19 10K R0201 5%
HDMII_RX_HPDOUT_M2
R22 10K R0201 5%
Q7 2SK3018 SOT_323

HPD:
Sink Side: Require output, Min 2.4V; Max 5.3V
Source Side:Require input and Detection.
Min 2.0V,Max:5.3V

VCC_1V8_S0
VCC5V_HDMIRX_PORT
R13 10K 5% R0201
R12 10K R0201 5%
HDMI_RX_DET_L
Q2 2SK3018 SOT_323

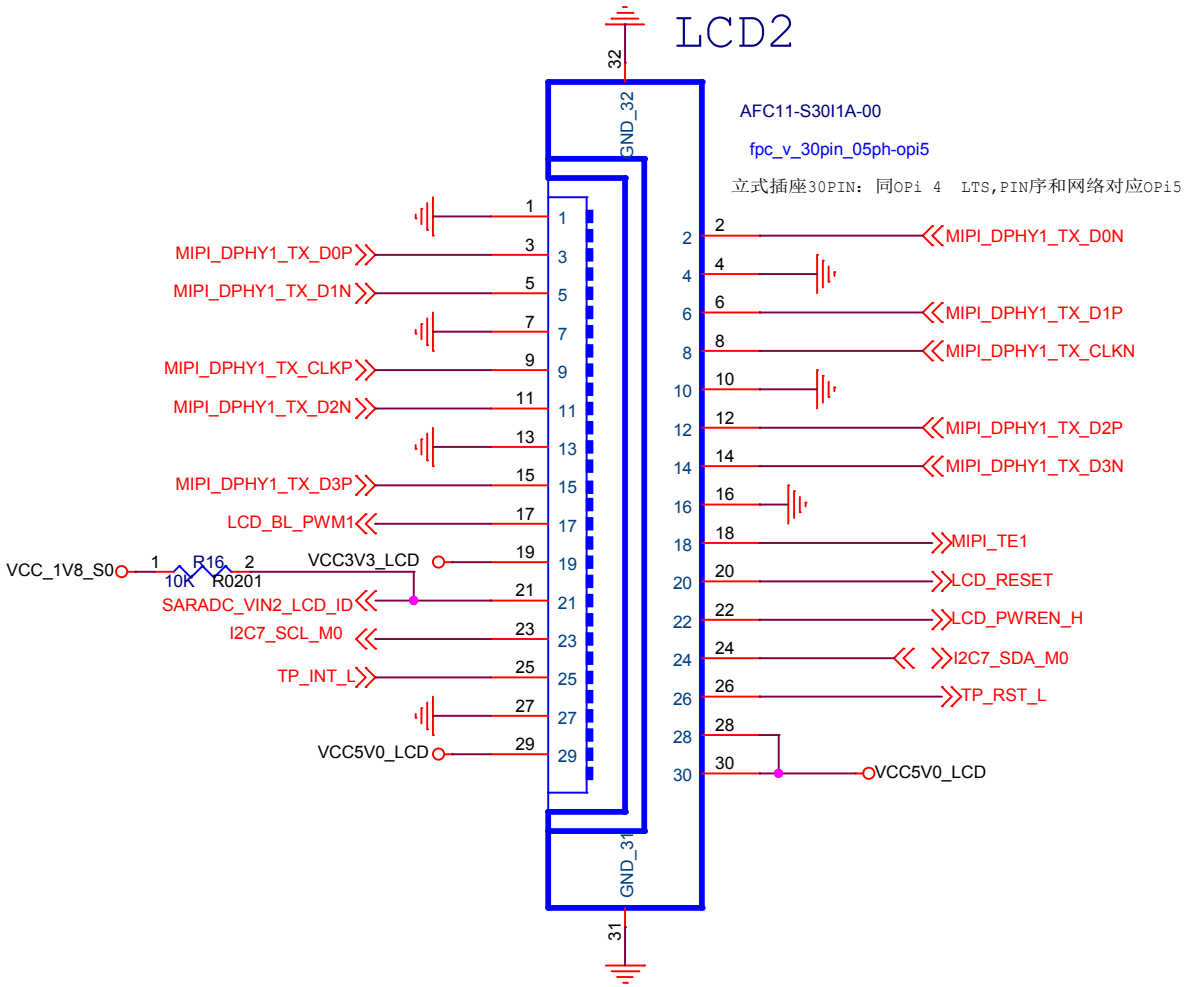
VCC_3V3_S0
R20 56K 5% R0201
Q15 2SK3018 SOT_323
R21 56K R0201 5%
HDMI_RX_CEC_M2 — HDMI_RX_CEC_PORT

Note:
(This HDMI2.0 RX interface has low probability anomalies, such as splash screen and restarts in scenarios such as frequent plug and pull, high and low resolution switching, etc. The probability is between 0.1% and 1%. We are still trying to debug and solve these problems. If the user will frequently use various peripherals to insert this HDMI2.0 RX interface, it is recommended to use external bridges connecting chips to improve compatibility to avoid affecting product production.)

HDMI_RX_D2P
HDMI_RX_D2N
HDMI_RX_D1P
HDMI_RX_D1N
HDMI_RX_D0P
HDMI_RX_D0N
HDMI_RX_CLKP
HDMI_RX_CLKN
HDMI_RX_CEC_PORT
HDMI_RXDDC_SCL_PORT
HDMI_RXDDC_SDA_PORT
VCC5V_HDMIRX_PORT
HDMI_RX_HPD_PORT
J1 HDMI_TYPE_A hdmi-type-a

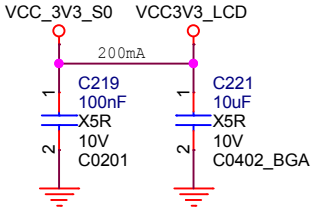
Shenzhen Xunlong Software Co., Ltd	
Project:	OPi 5 Ultra
File:	34.VO-HDMI2.1 TX/RX
Date:	Monday, January 13, 2025
Rev:	V1.0
Size:	A3
Sheet:	25
Of:	28

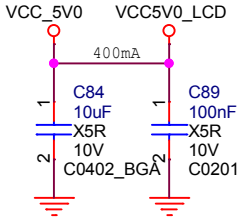
MIPI DPHY1 TX



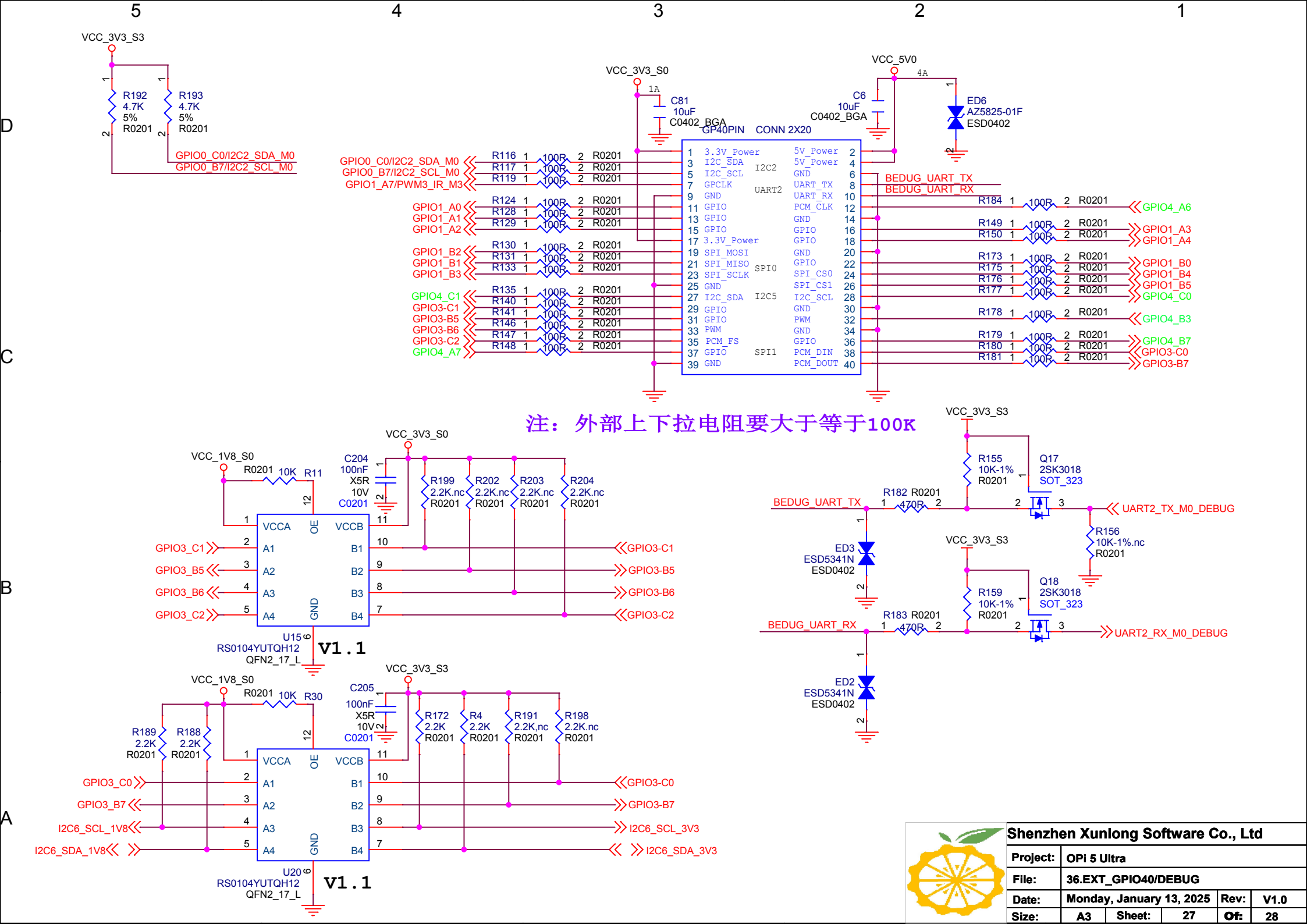
FPC Pin List

Pin1 :GND
Pin2 :D0N
Pin3 :D0P
Pin4 :GND
Pin5 :D1N
Pin6 :D1P
Pin7 :GND
Pin8 :CLKN/AUXN
Pin9 :CLKP/AUXP
Pin10:GND
Pin11:D2N
Pin12:D2P
Pin13:GND
Pin14:D3N
Pin15:D3P
Pin16:GND
Pin17:LCD_PWM_BL
Pin18:LCD_TE
Pin19:VCC3V3_LCD
Pin20:LCD_RST
Pin21:LCD_ID
Pin22:LCD_PWREN
Pin23:TP_I2C_SCL
Pin24:TP_I2C_SDA
Pin25:TP_INT
Pin26:TP_RST
Pin27:GND
Pin28:5V0
Pin29:5V0
Pin30:5V0





Shenzhen Xunlong Software Co., Ltd					
Project:	OPi 5 Ultra				
File:	35.VO-LCM_MIPI				
Date:	Monday, January 13, 2025			Rev:	V1.0
Size:	A3	Sheet:	26	Of:	28


5
4
3
2
1
D
C
B
A
VCC_3V3_S3
R192 4.7K 5% R0201
R193 4.7K 5% R0201
GPIO0_C0/I2C2_SDA_M0
GPIO0_B7/I2C2_SCL_M0
VCC_3V3_S0
1A
C81 10uF C0402_BGA
GP40PIN CONN 2X20
VCC_5V0
4A
C6 10uF C0402_BGA
ED6 AZ5825-01F ESD0402
BEDUG_UART_TX
BEDUG_UART_RX
GPIO1_A0
GPIO1_A1
GPIO1_A2
GPIO1_B2
GPIO1_B1
GPIO1_B3
GPIO4_C1
GPIO3-C1
GPIO3-B5
GPIO3-B6
GPIO3-C2
GPIO4_A7
GPIO4_A6
GPIO1_A3
GPIO1_A4
GPIO1_B0
GPIO1_B4
GPIO1_B5
GPIO4_C0
GPIO4_B3
GPIO4_B7
GPIO3-C0
GPIO3-B7
注：外部上下拉电阻要大于等于100K
VCC_1V8_S0
VCC_3V3_S0
C204 100nF X5R 10V C0201
R199 2.2K.nc R0201
R202 2.2K.nc R0201
R203 2.2K.nc R0201
R204 2.2K.nc R0201
U15 RS0104YUTQH12 QFN2_17_L
V1.1
VCC_3V3_S3
C205 100nF X5R 10V C0201
R172 2.2K R0201
R4 2.2K R0201
R191 2.2K,nc R0201
R198 2.2K.nc R0201
R189 2.2K R0201
R188 2.2K R0201
I2C6_SCL_1V8
I2C6_SDA_1V8
I2C6_SCL_3V3
I2C6_SDA_3V3
U20 RS0104YUTQH12 QFN2_17_L
V1.1
R155 10K-1% R0201
Q17 2SK3018 SOT_323
R182 R0201 470R
UART2_TX_M0_DEBUG
R156 10K-1%.nc R0201
ED3 ESD5341N ESD0402
R159 10K-1% R0201
Q18 2SK3018 SOT_323
R183 R0201 470R
UART2_RX_M0_DEBUG
ED2 ESD5341N ESD0402
Shenzhen Xunlong Software Co., Ltd
Project: OPi 5 Ultra
File: 36.EXT_GPIO40/DEBUG
Date: Monday, January 13, 2025
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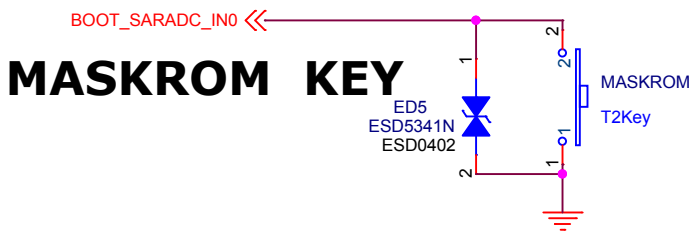
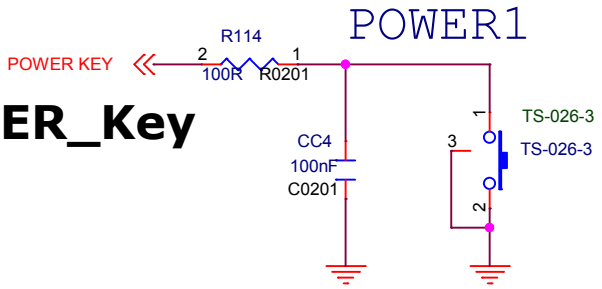
5 4 3 2 1

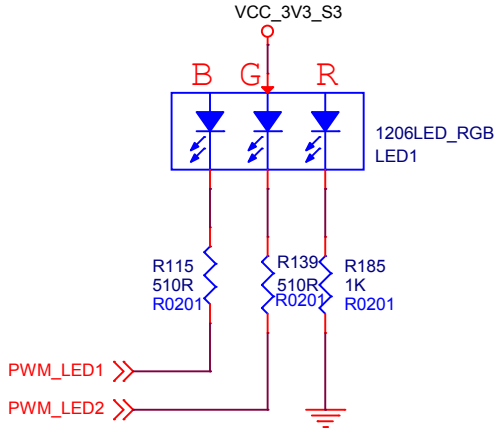
D C B A

BOOT



POWER1





Shenzhen Xunlong Software Co., Ltd					
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File:	37 KEY/LED				
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